X fest

PRESENTED BY

AVNET

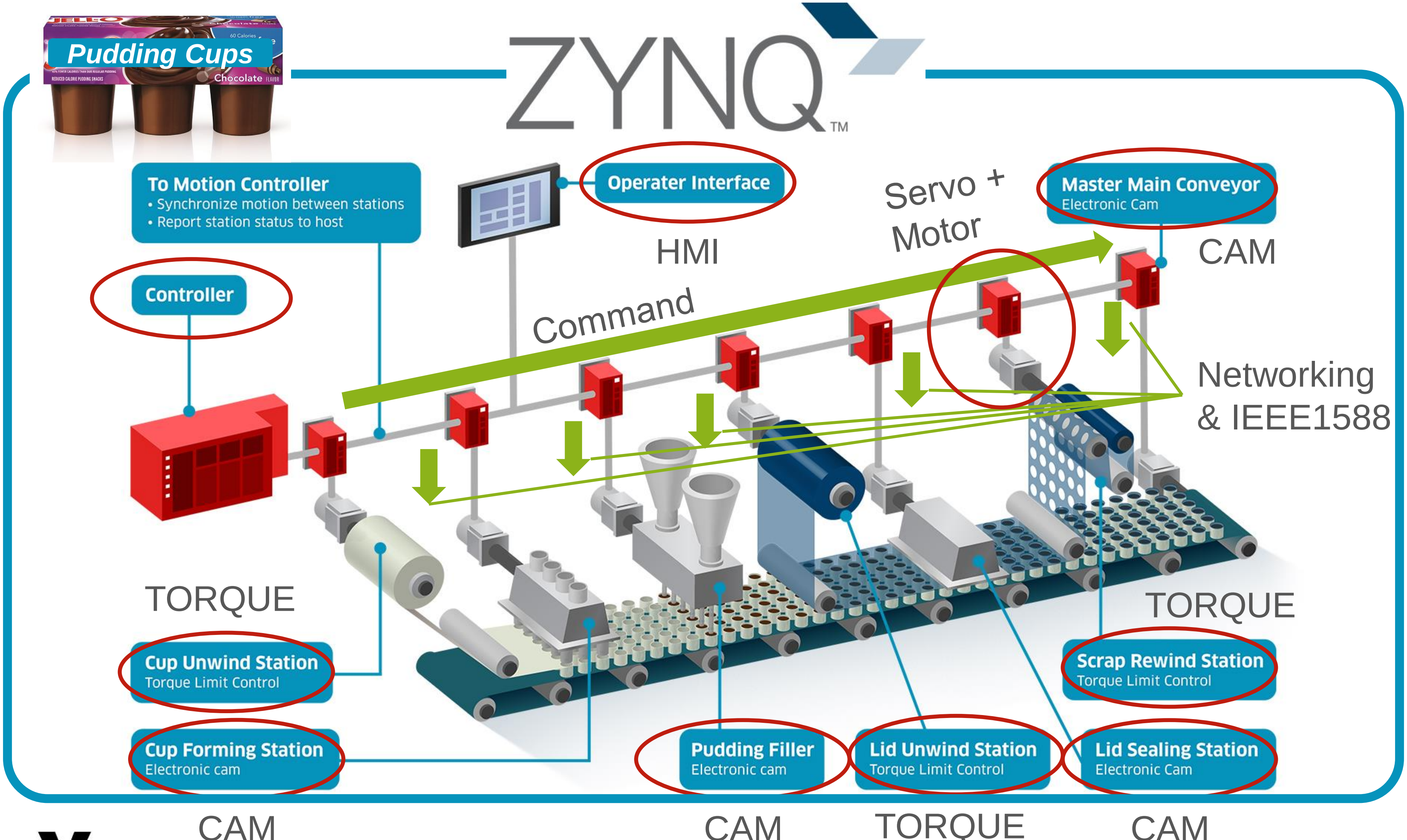
Matt Brown

Zynq Intelligent Drives

Motor Control with Industrial Ethernet and Functional Safety

Accelerating Your Success™

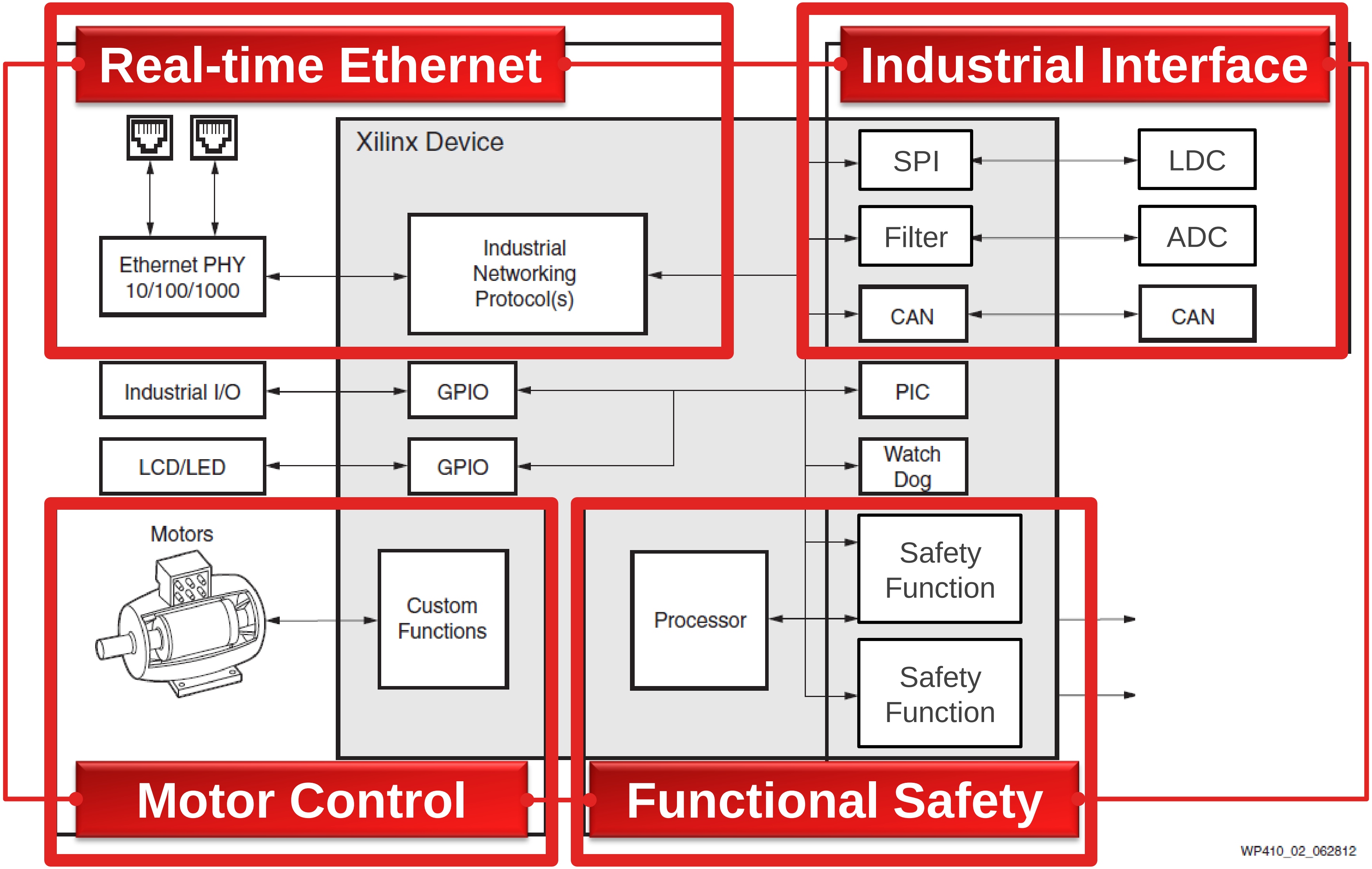
Example of Electrical Drives in Pudding Production



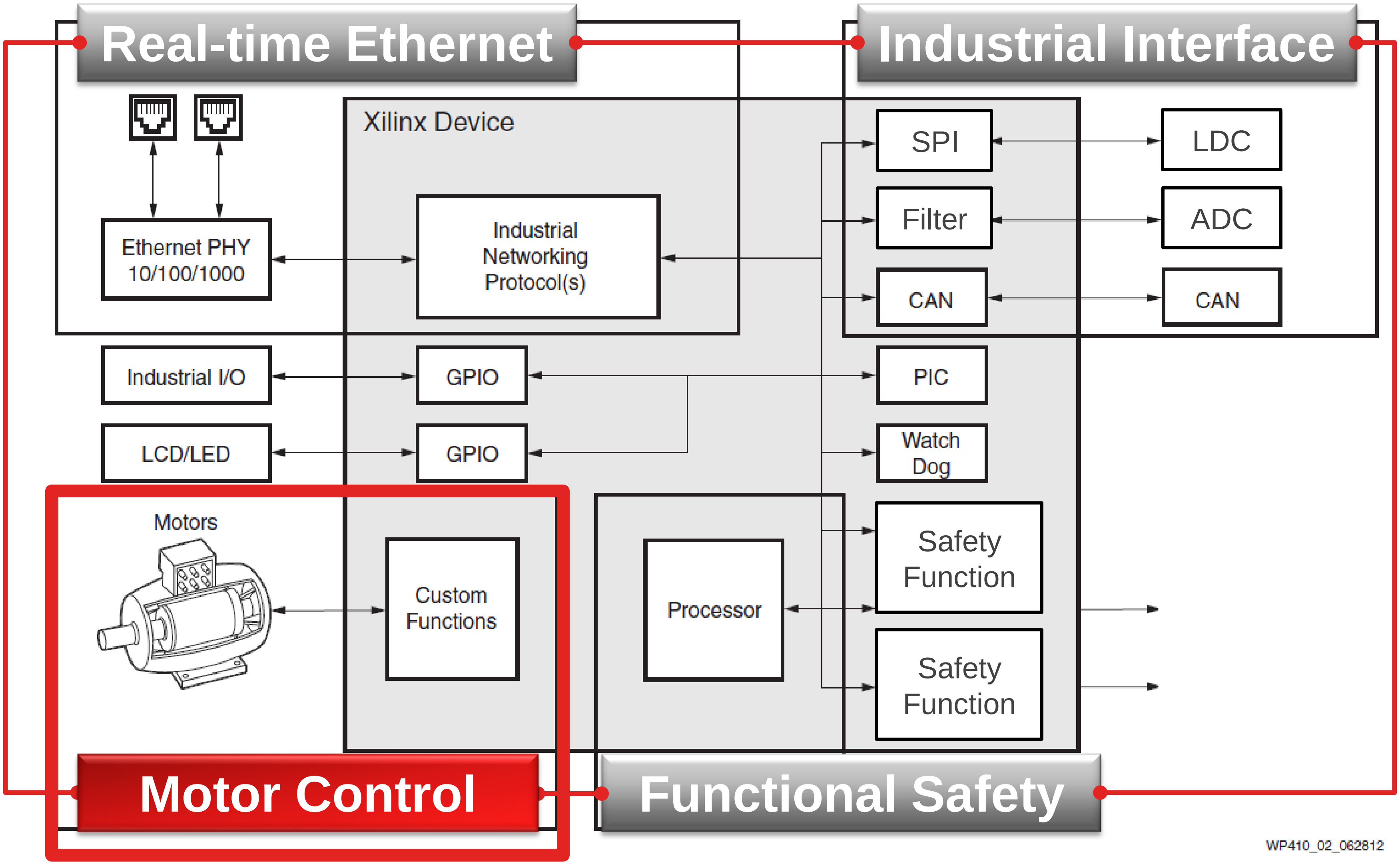
Course Objectives

- Explore system simulation, code generation, and prototype of motor control algorithms using MATLAB® and Simulink® with Avnet's Zynq Intelligent Drives Kit
- Investigate how Zynq enables multiple real-time Industrial Ethernet protocols
- Understand how multi-channel fault tolerant systems can be implemented in a single programmable device
- Learn about innovative high precision industrial sensing, signal acquisition, and interface solutions

Agenda


Real-time Ethernet
Industrial Interface
Xilinx Device
Ethernet PHY 10/100/1000
Industrial Networking Protocol(s)
SPI
Filter
CAN
LDC
ADC
CAN
Industrial I/O
GPIO
PIC
LCD/LED
GPIO
Watch Dog
Motors
Custom Functions
Processor
Safety Function
Safety Function
Motor Control
Functional Safety
WP410_02_062812

Agenda



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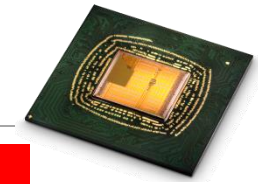
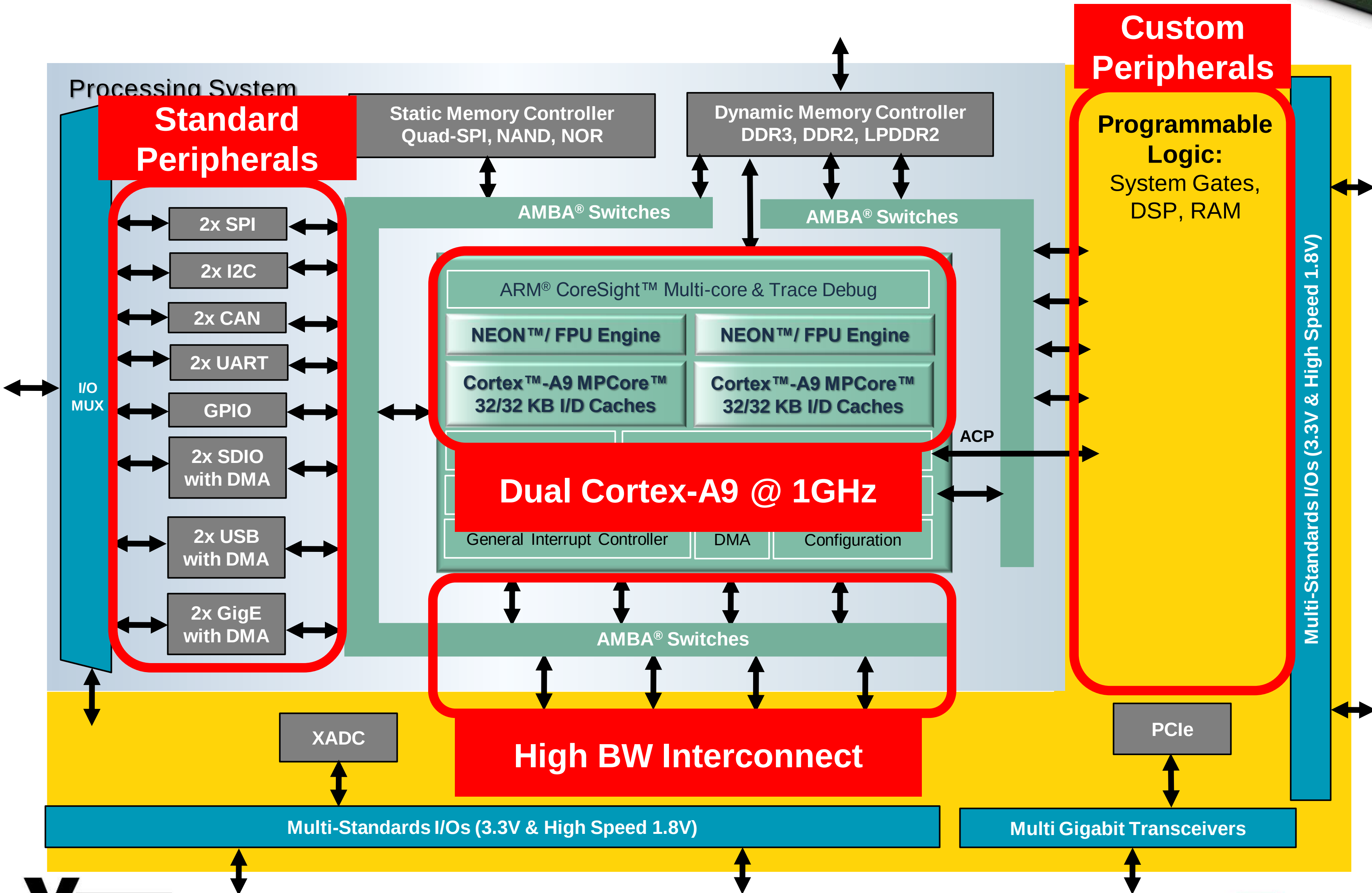
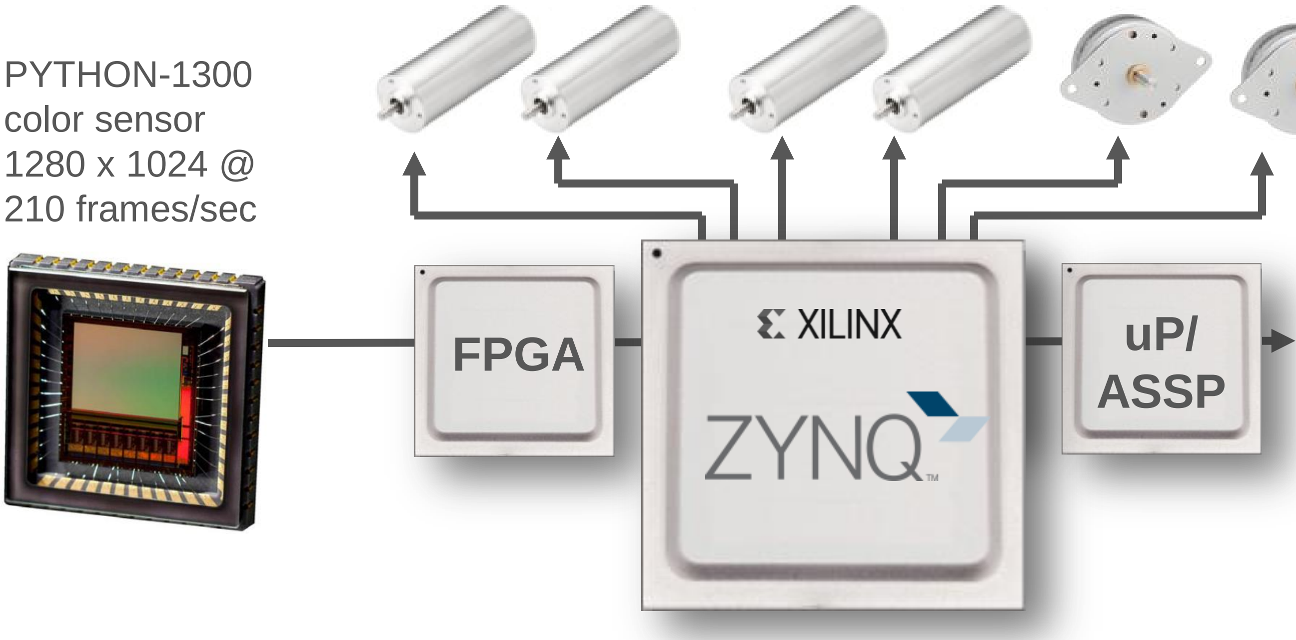
Zynq-7000 Family Highlights





Zynq Delivers Unprecedented Integration

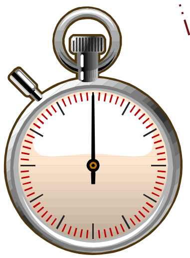
PYTHON-1300
color sensor
1280 x 1024 @
210 frames/sec



- One scalable platform for all products
- Flexible support of multiple protocols
- Lower system power
- Higher reliability / better MTBF

Advanced Control Algorithms Require Fast Loops

ZYNQ FPGA: 1.6us



MCU: 55-100us

+30x faster control loop means better precision, greater performance and higher efficiency

Clarke Transform:
Convert phase currents from 3-axis to 2-axis

ParkTransform:
Convert to rotating coordinate system

Slide Mode Controller:
Estimate motor position and speed

PI Controllers:
Estimate and correct error in speed & torque

Inverse Park Transform:
Convert rotating to stationary coordinates

Inverse Clarke Transform:
Convert 2-axis to 3-axis

Power Modulation:
PWM, SVM, RPFM

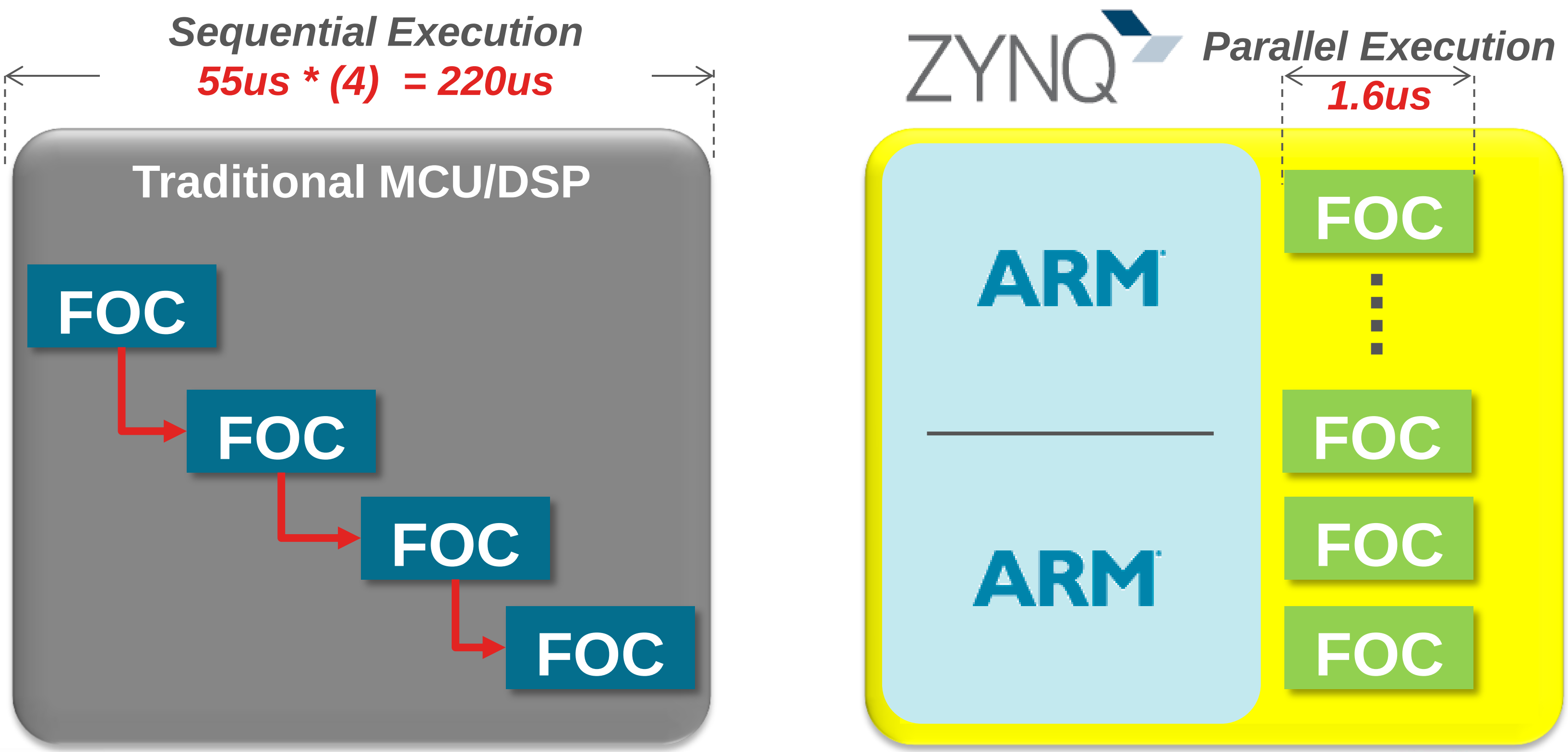
ADC

Sensorless Field Oriented Control

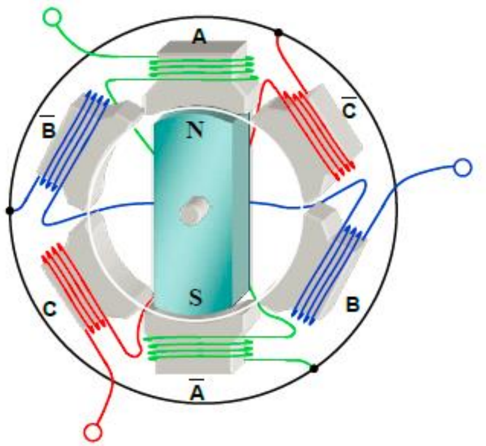
Drive Stage

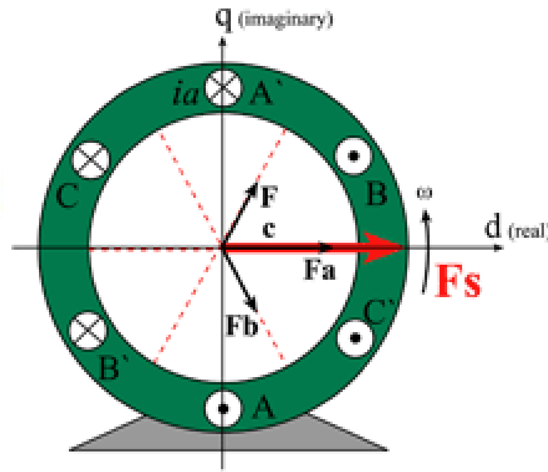
Zynq Delivers Unprecedented Performance

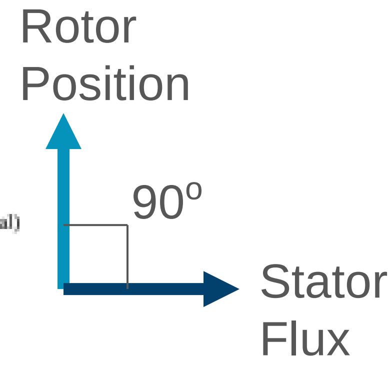
- Advanced algorithms require fast, deterministic processing
- Field Oriented Control (FOC) loops suffer sequential delay in MCU
- Zynq is scalable to any number of motors with no performance loss

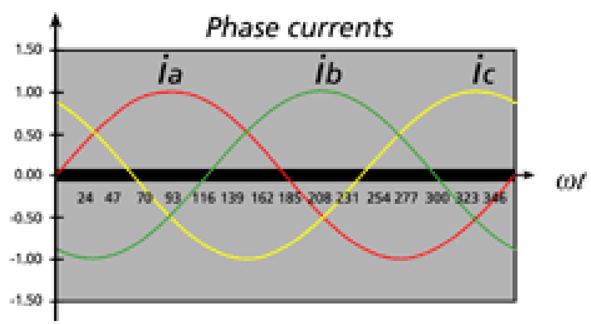


Controllers Must Generate a Rotating Field



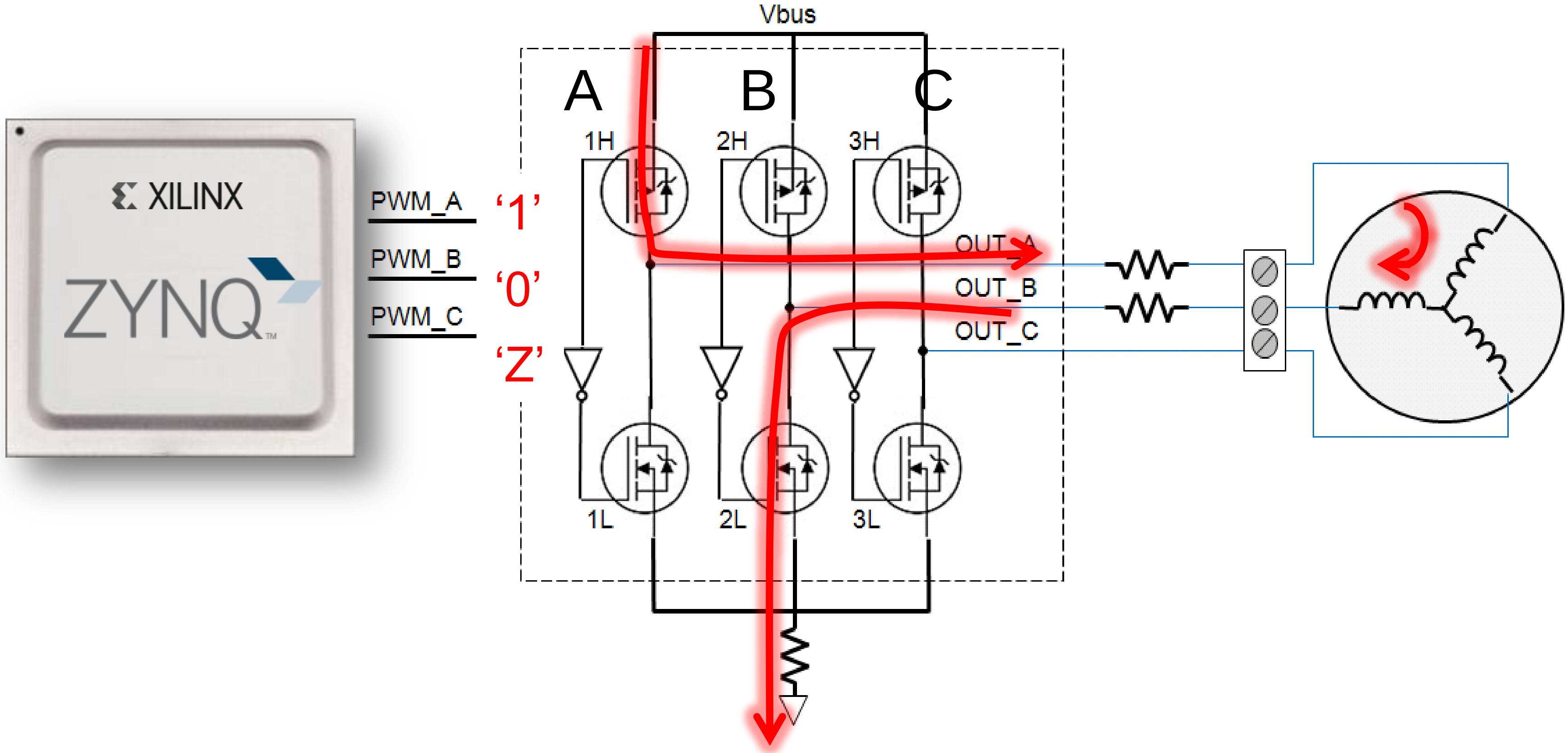






- **Alternating currents in stator windings create rotating field**
- **Rotor with permanent magnet follows rotating field**
- **Maximum torque when magnet flux angle is 90° from rotor**

Typical 3-phase Power Stage is Limited



- PWM creates binary (on/off) voltage from h-bridge
- Torque profile is not smooth unless more sophisticated control methods are implemented

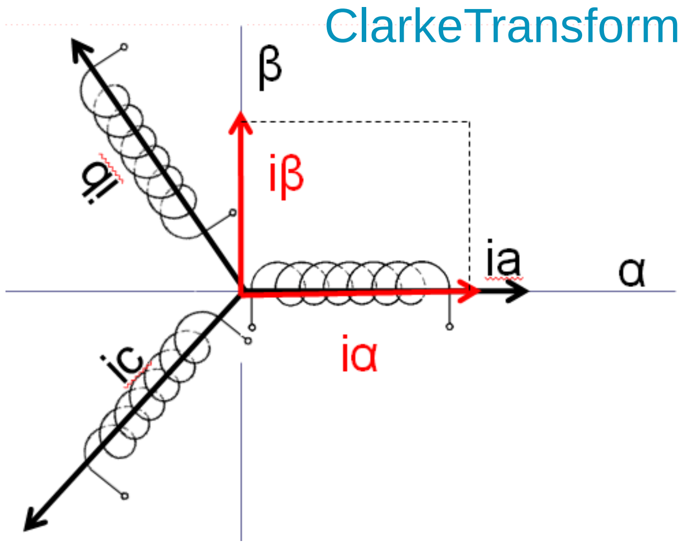
Field Oriented Control for Precise Motor Torque

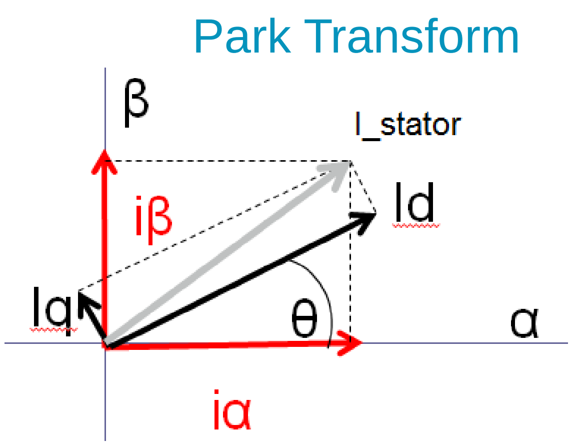
- Measuring and controlling the motor in vector space
- Map three phase stator currents into two dimensions (α,β)

  ia + ib + ic = 0
  iα = ia
  iβ = (ia +2ib)/√ 3

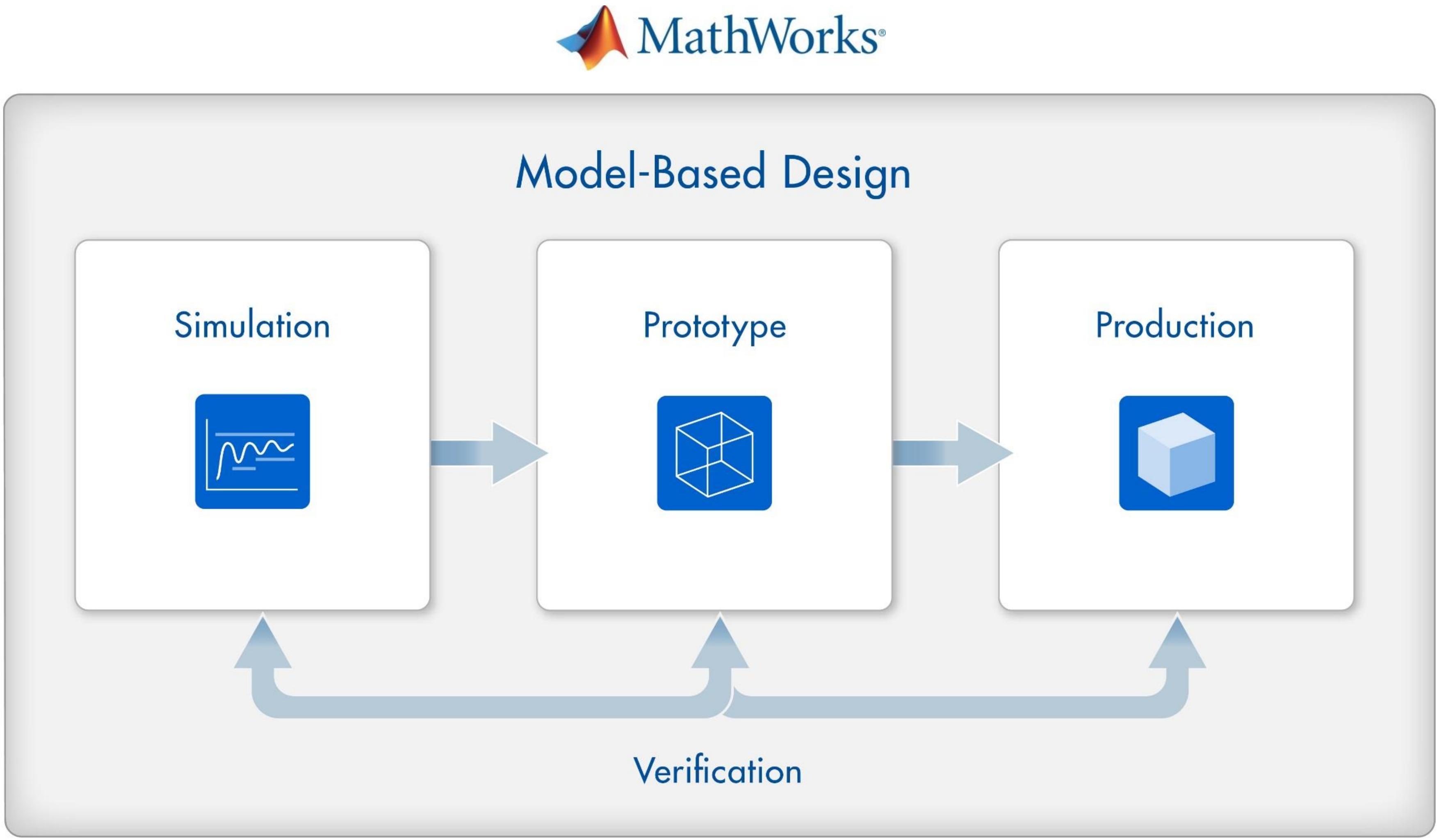
- Map the two phase orthogonal system (α,β) into the rotating reference frame (d, q)

  Id = iα cosθ + iβ sinθ → rotor flux
  Iq = -iα sinθ + iβ cosθ → torque

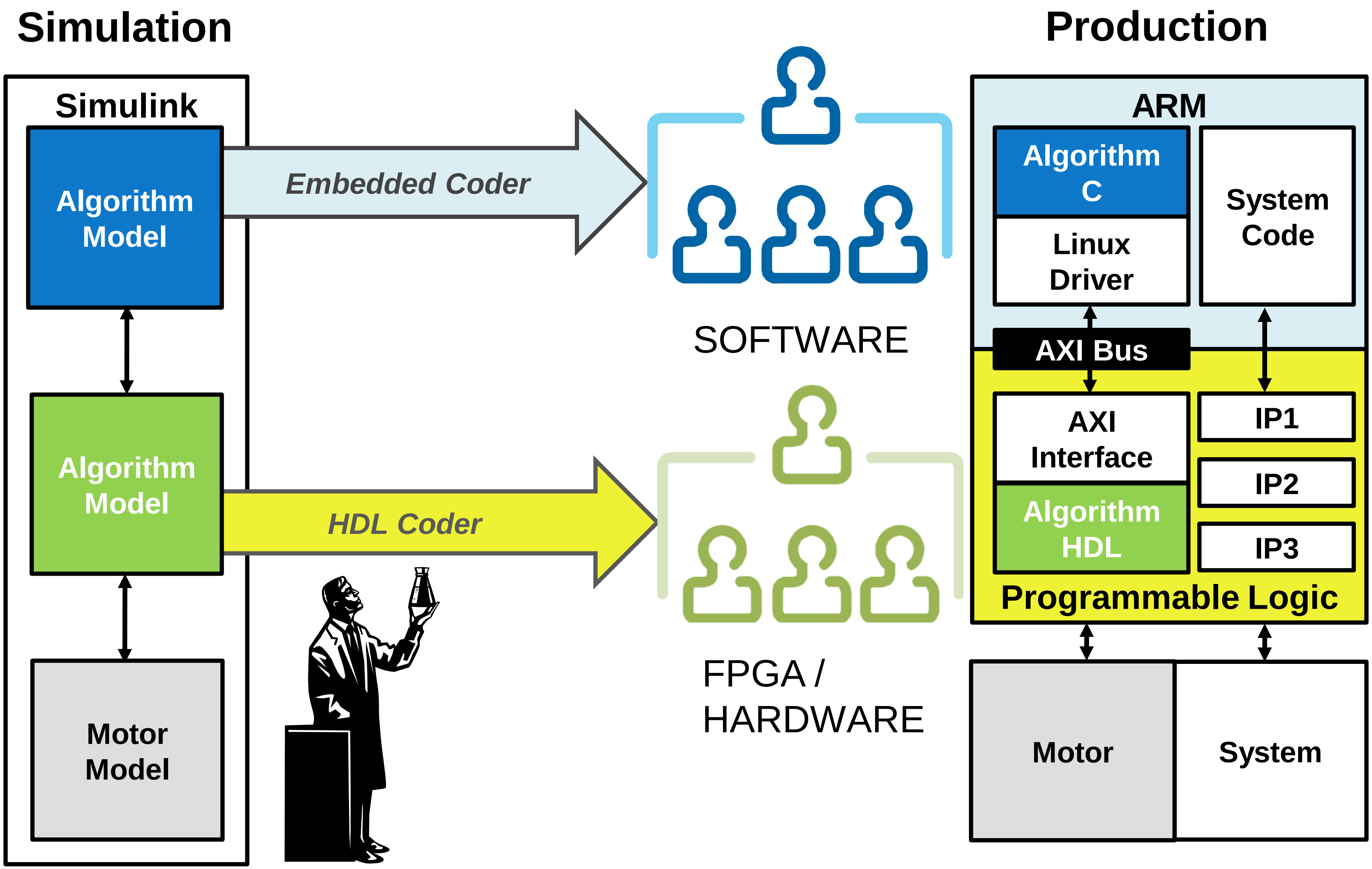




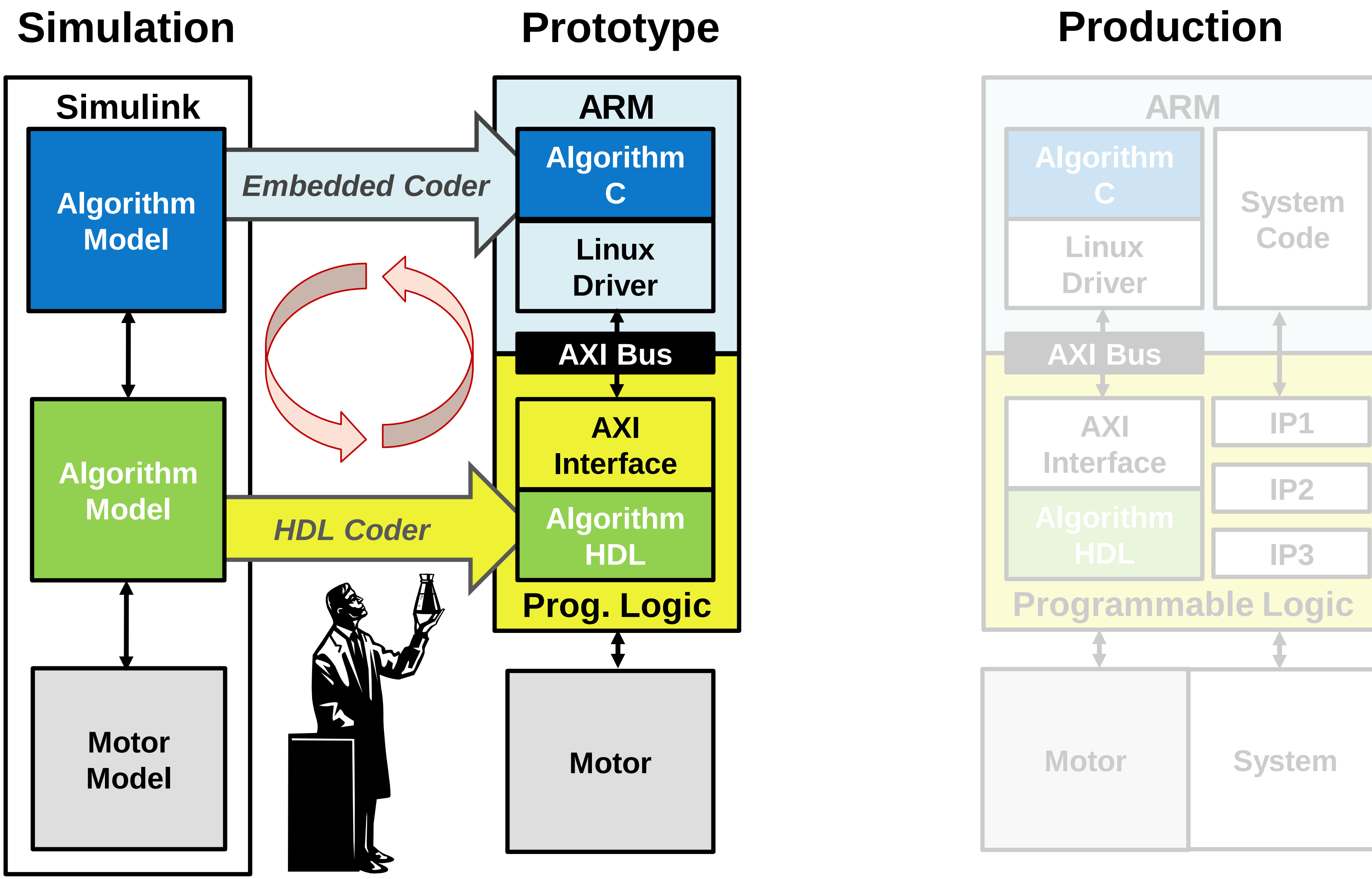
Model-Based Design with MATLAB and Simulink



Challenge of Hardware Prototyping



Zynq Support Package Accelerates Prototyping

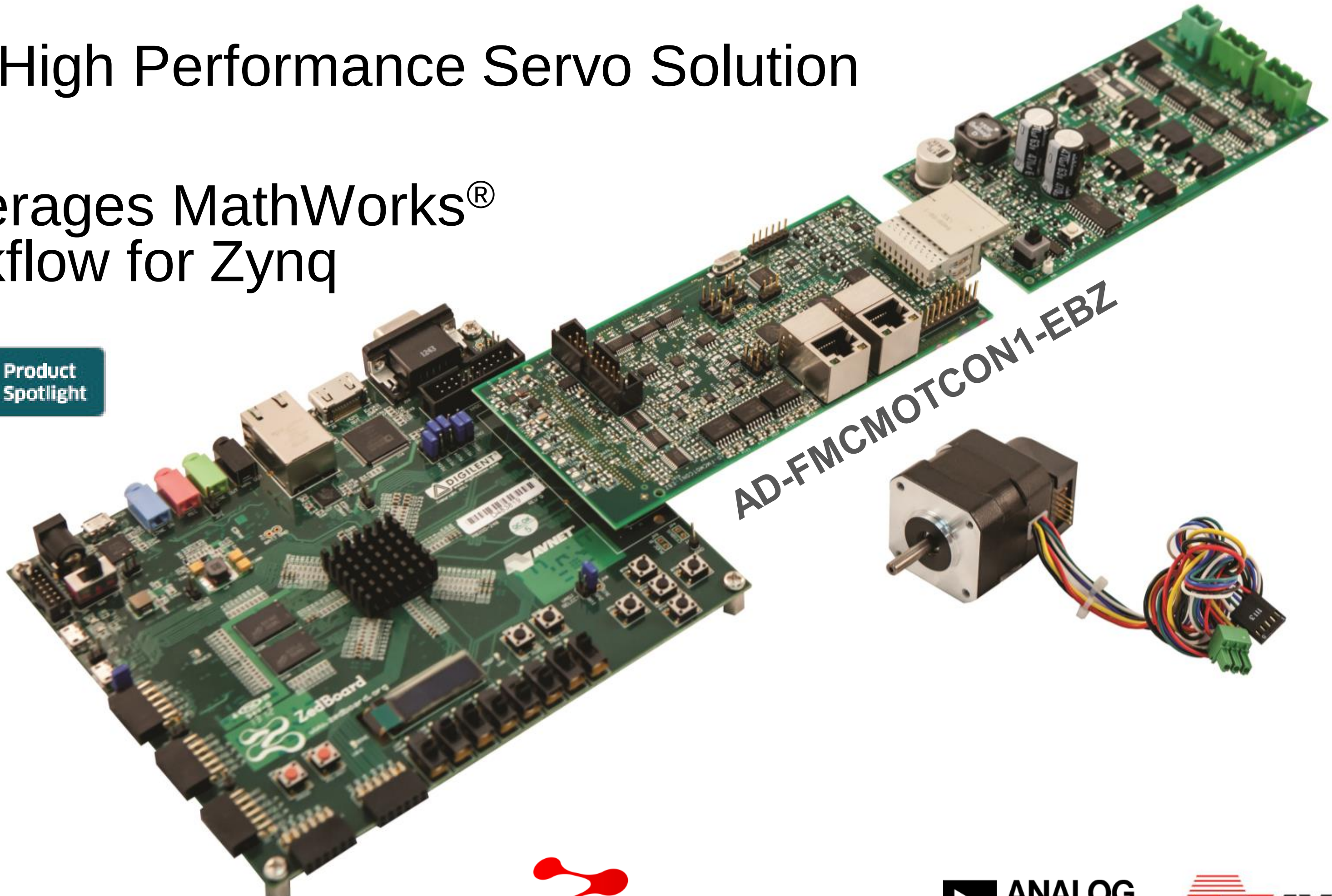


Zynq-7000 AP SoC / Analog Devices Intelligent Drives Kit

Zynq-7000 AP SoC / Analog Devices Intelligent Drives Kit

- Features ZedBoard low-cost community baseboard
- ADI High Performance Servo Solution
- Leverages MathWorks® workflow for Zynq

Xfest Product Spotlight



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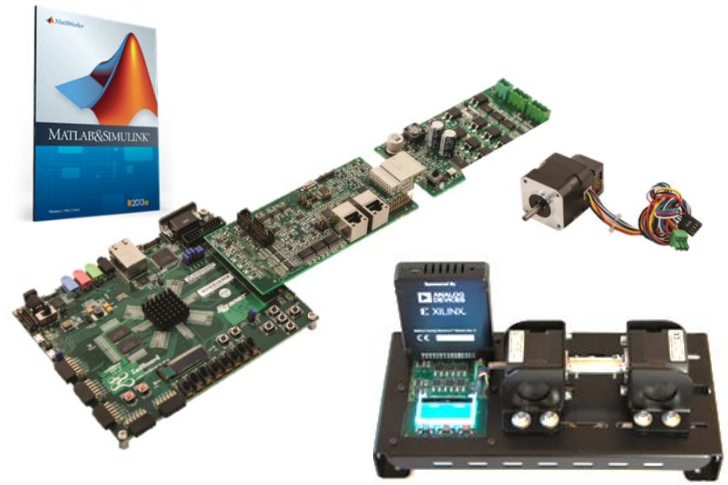
ZedBoard.org ANALOG DEVICES AVNET

Kit Features

- Function
  - Drive BDC, BLDC, PMSM, Stepper motors up to 48V @ 18A
  - ADI isolation for power and signals
  - AD7401A isolated ΣΔ data converters
  - XADC connection
  - Dual Gigabit IEEE1588 Ethernet
  - 8GB SD Card
- Linaro® Linux framework with Field Oriented Controller from MathWorks
- Xilinx Vivado Design Edition voucher
- MathWorks Motor Control Design Package *(optional)*

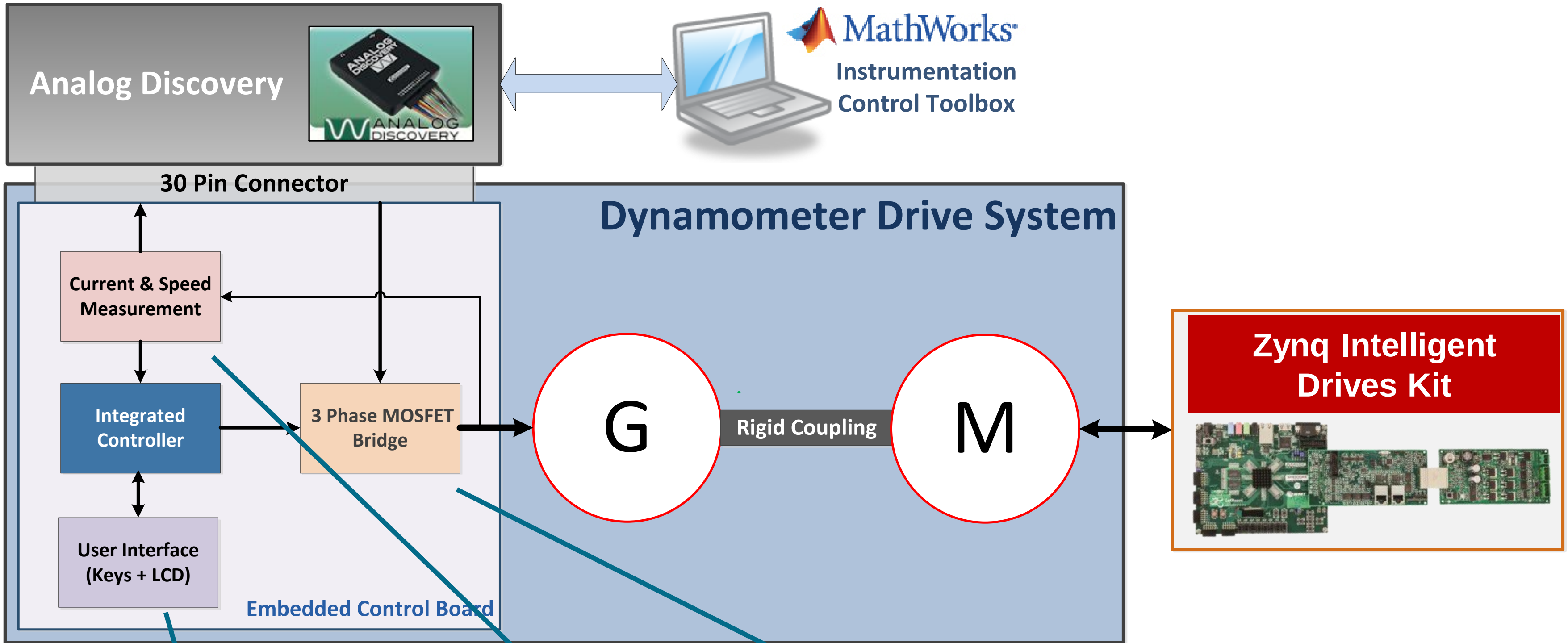


em.avnet.com/zynq7000idk

Base Kit
AES-ZIDK-ADI-G **$995**

Base Kit + Dynamometer
AES-ZIDK-ADI-DYNO-G **$1695**

Dynamometer Block Diagram

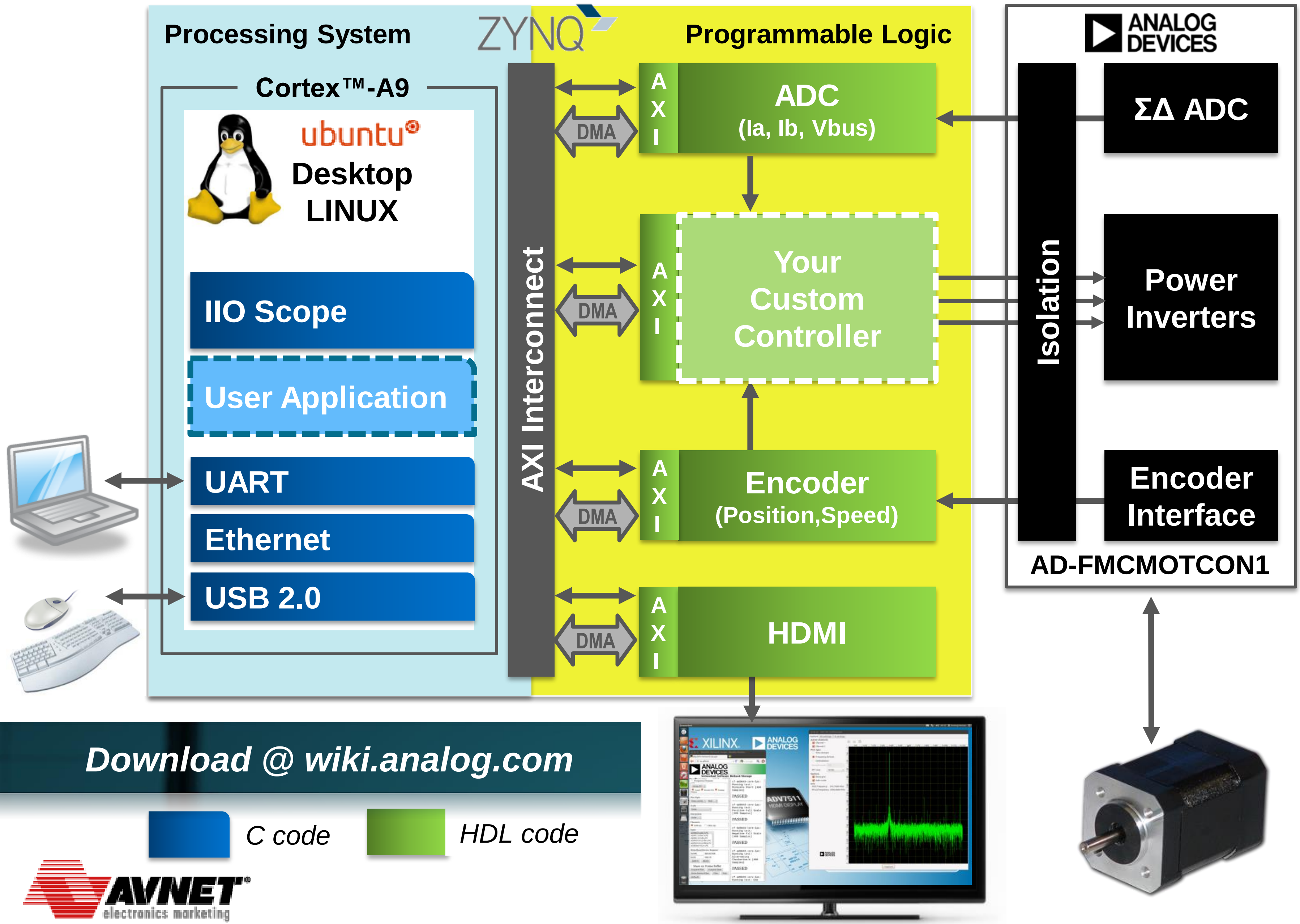


3-phase MOSFET bridge adjusts generator load

User Interface to change load profiles and view speed/current

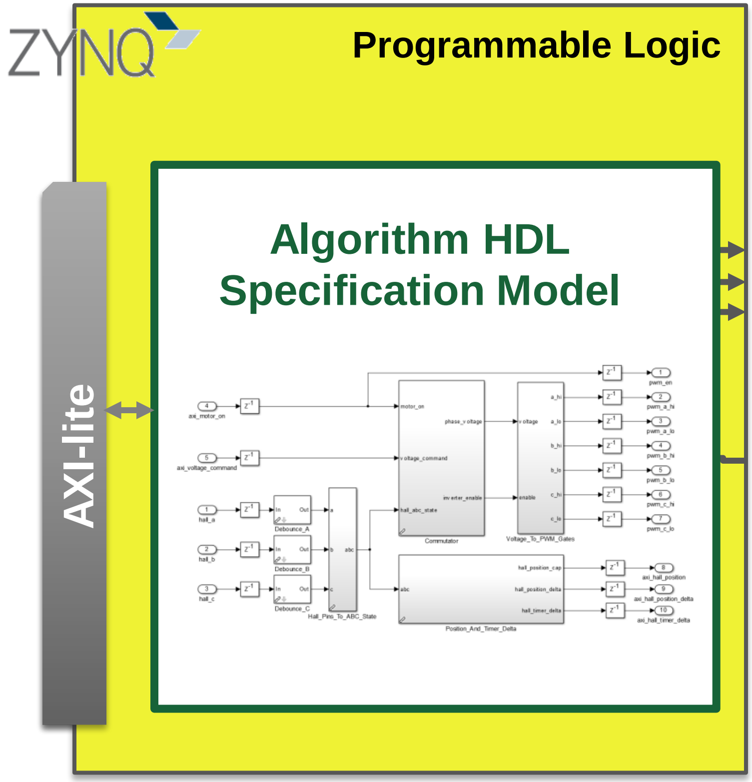
Measure signals and control load using Analog Discover Module with MATLAB

ADI Base Reference Design Architecture



MathWorks Prototype on Zynq

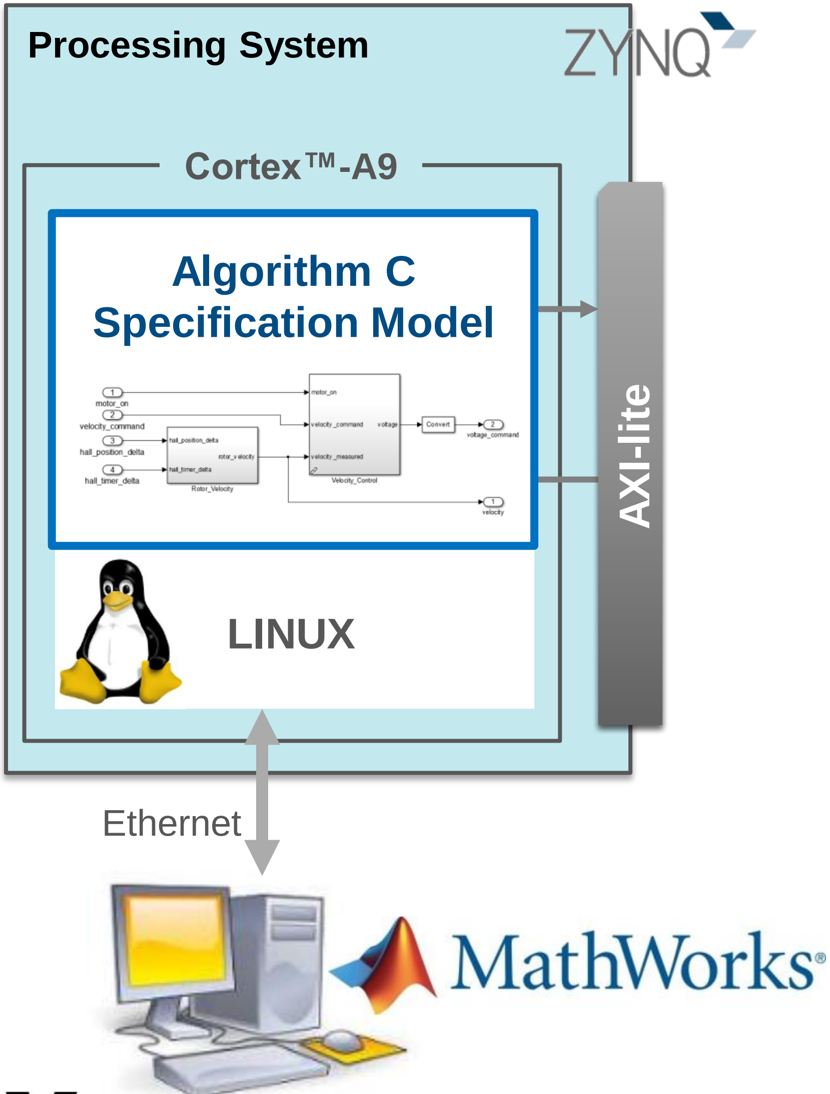
MathWorks Zynq Support Package



Automatically …

- Generate algorithmic HDL code from Simulink models, including interfaces to the AXI4 bus and devices pins
- Compile and load a bitstream into the programmable logic

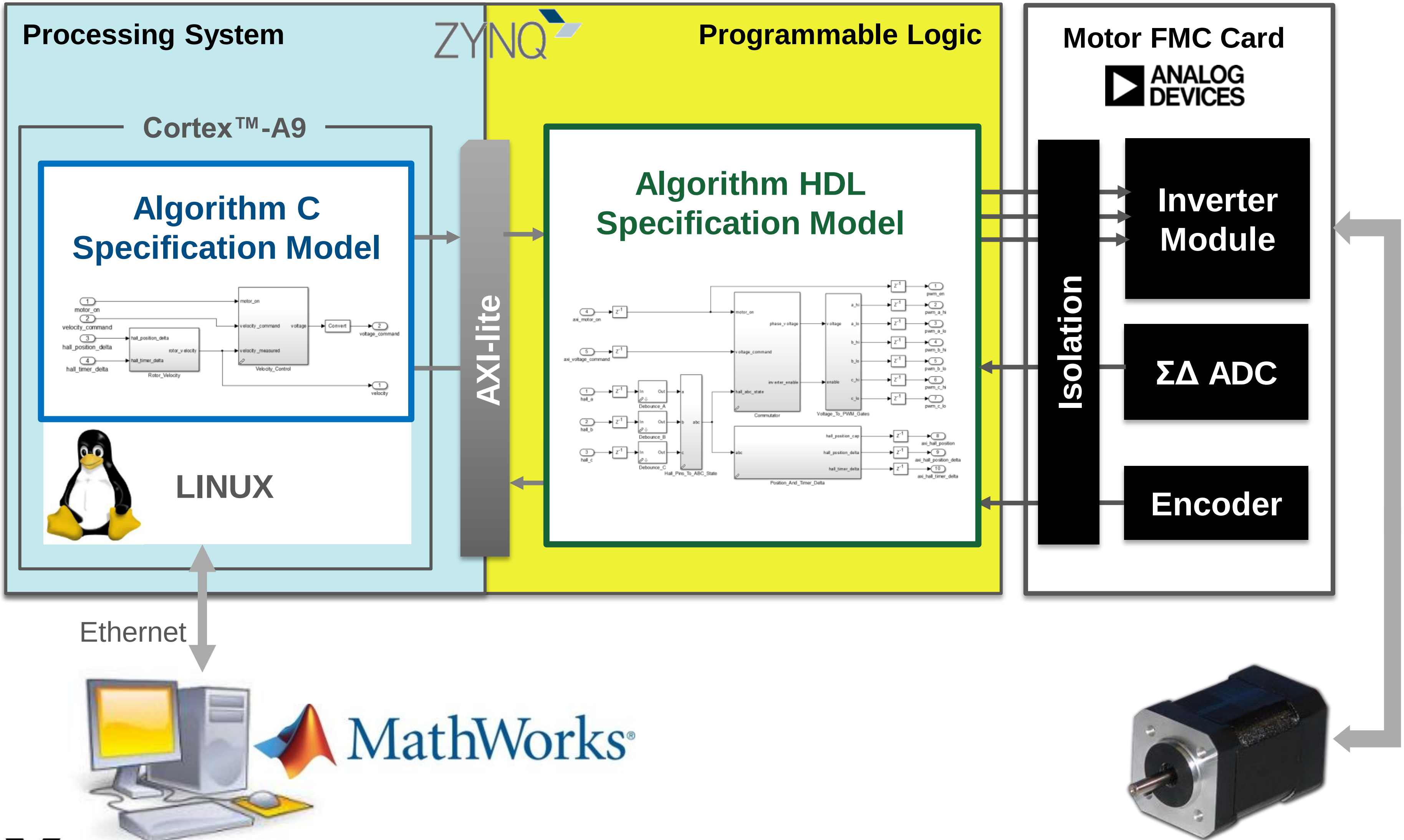
MathWorks Zynq Support Package



Automatically …

- Generate ARM executable consisting of algorithmic C code from models and interfaces to AXI-Bus
- Algorithm C code executes in the user space of Linux
- AXI4-Lite SW driver is automatically created and inserted
- Interface between Simulink and ARM executable via Ethernet (External Mode)

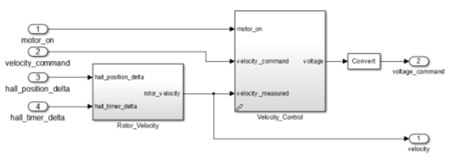
Simulink Motor Control Model Prototyped on Zynq



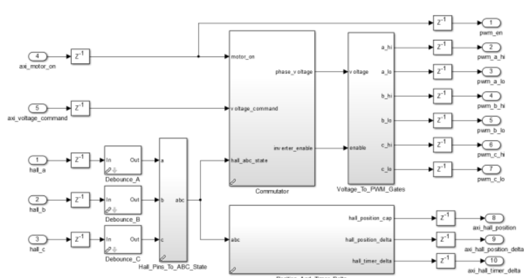
From Simulation to Prototype to Production

Simulation

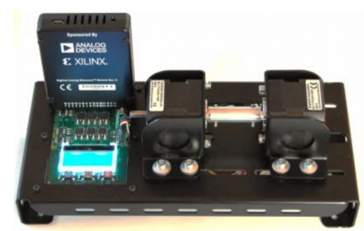
Algorithm C Specification Model



Algorithm HDL Specification Model



Prototype



VIVADO Production

ARM

Algorithm C

Linux Driver

System Code

AXI Bus

AXI Interface

Algorithm HDL

IP1

IP2

IP3

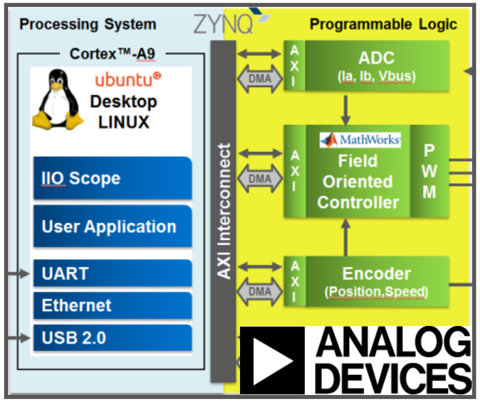
Programmable Logic

Motor

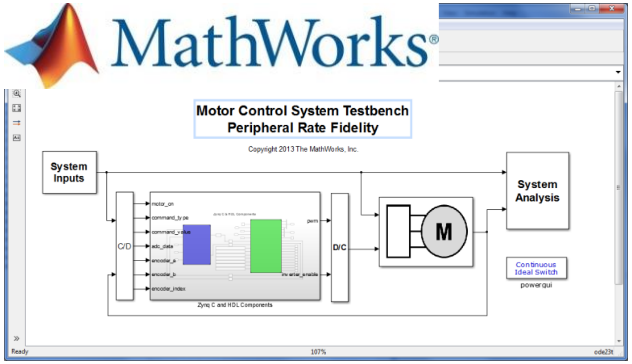
System

Motor Control Reference Designs and IP

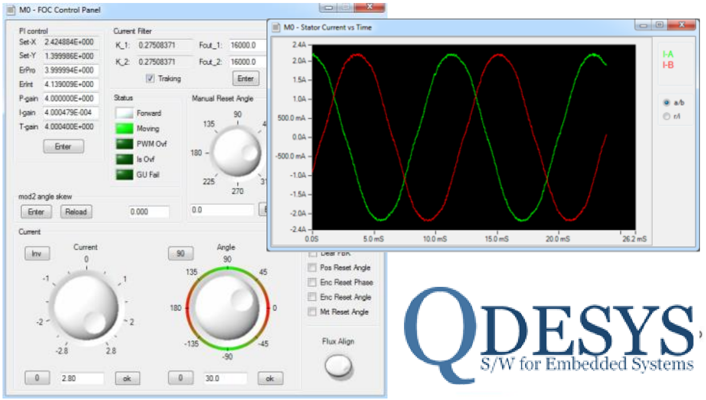
- **Analog Devices Reference Designs**
  - wiki.analog.com
  - Full C/HDL/Linux source



- **Explore Zynq Support Packages and Simulink Motor Control Models**
  - www.mathworks.com/zidk
  - Motor Control Design Package



- **High-performance IP from QDESYS**
  - www.qdesys.com
  - Sensorless Field Oriented Control
  - Instrumentation GUI and APIs
  - RPFM algorithm for max. efficiency



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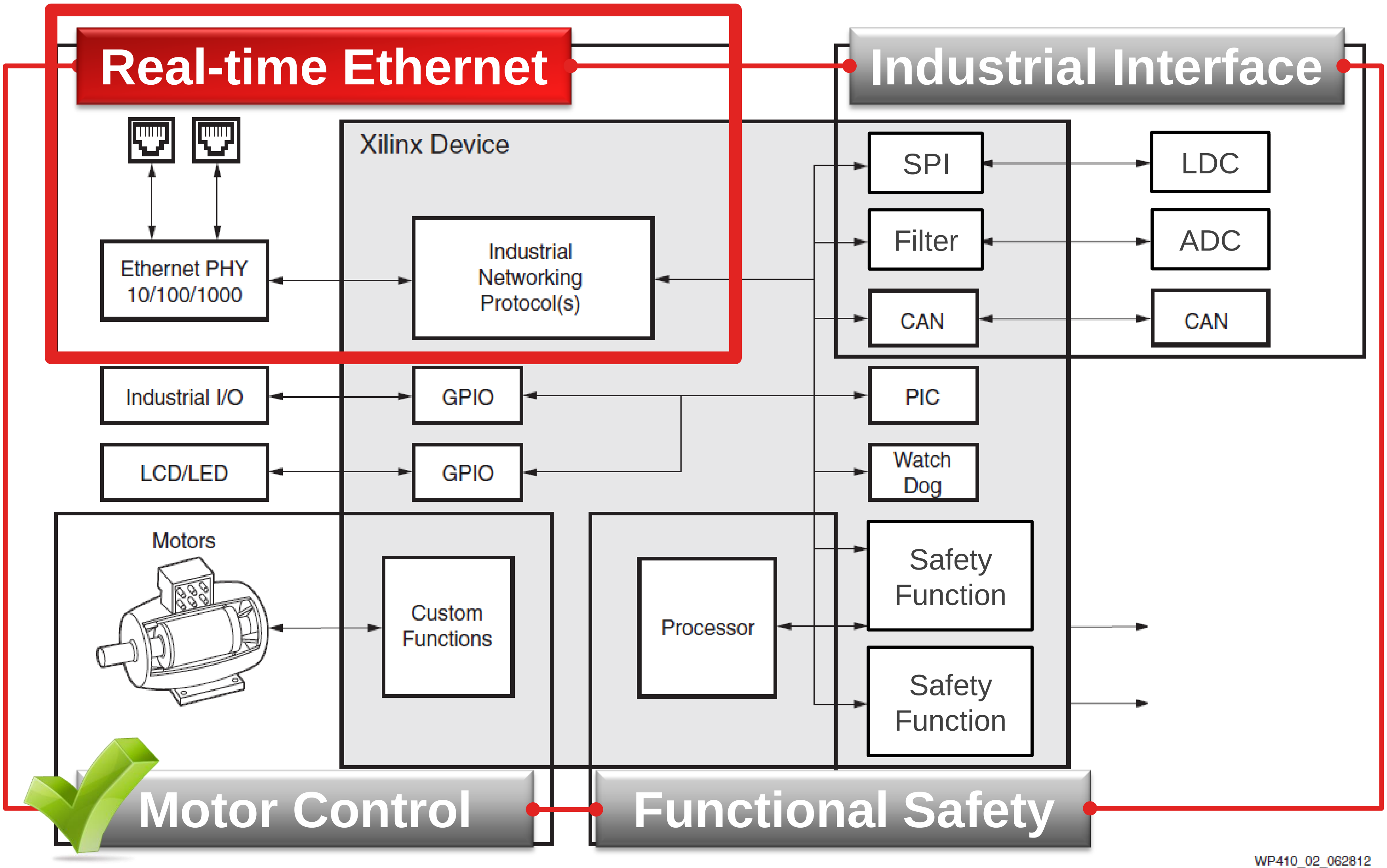
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Evolution of Fieldbus to Real-time Ethernet

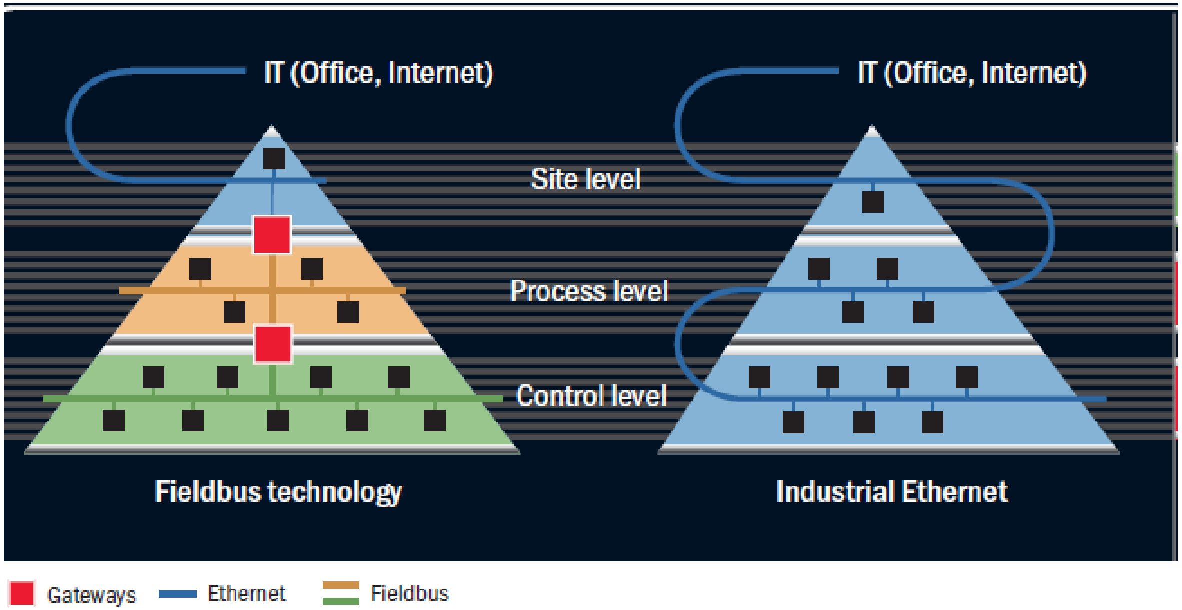
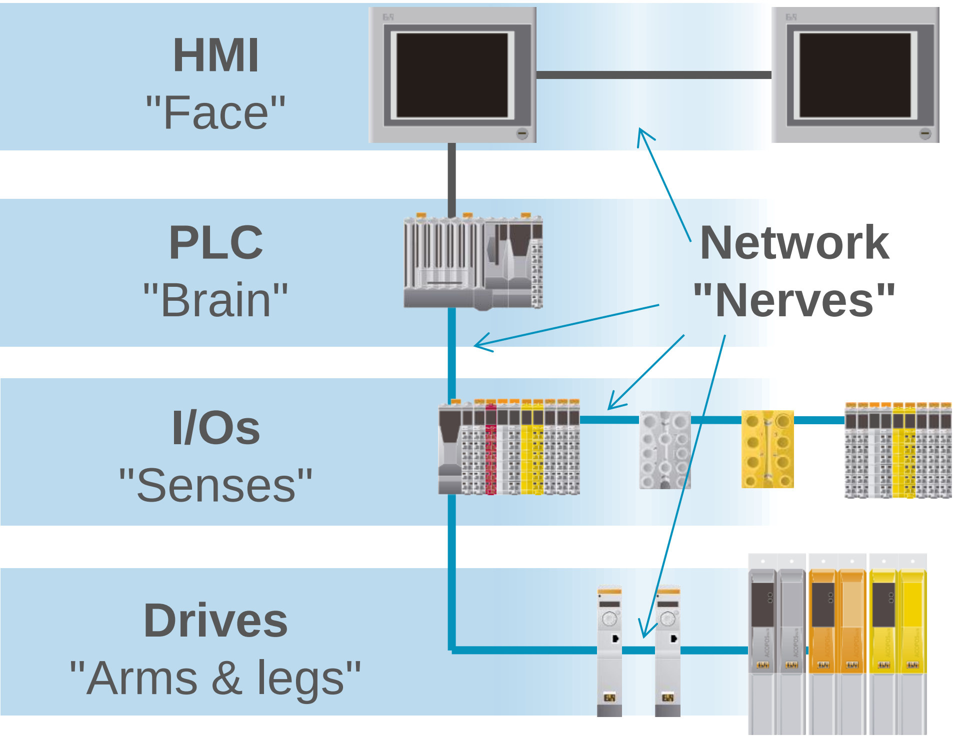


Image source: Ethernet POWERLINK Standardization Group (EPSG); publication MM-E01106.873; "Powerlink Basics"

- Traditional Fieldbus technology limits performance
- Ethernet creates open, flexible, high BW networks
- Real-time Ethernet adds determinism

Network Requirements in Smarter Factories



- **Determinism**
  - Fast reaction (in µs range)
  - Low jitter (in 100 ns range)
- **High performance**
  - Fast cycles (in 100 µs range)
  - Data transfer ranging from single Bytes (I/Os) to kBytes (vision systems)
- **Standardized**
  - Runs on IT infrastructure
  - Easy to diagnose
- **Scalable, Modular Systems**
  - Industrial devices and systems are interchangeable
  - Interoperable

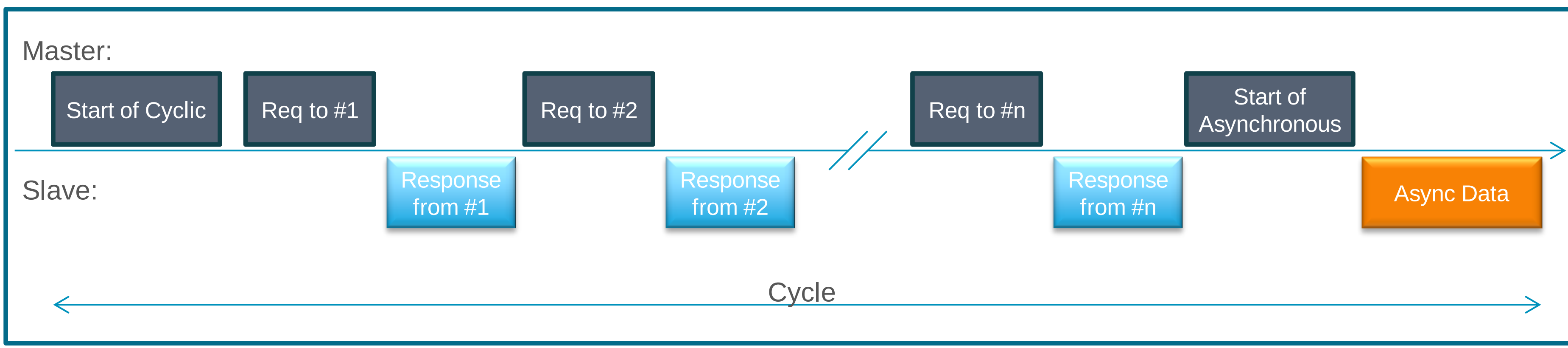
Case Study – POWERLINK on Zynq

POWERLINK protocol

- Use IEEE 802.3 Fast Ethernet

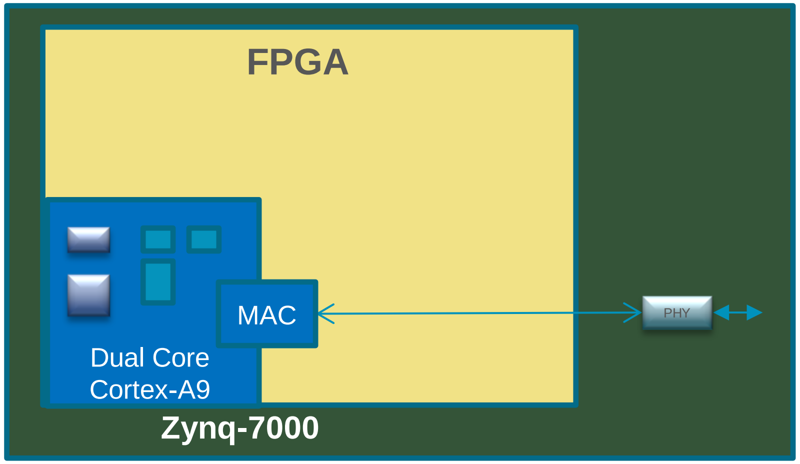
7B	1B	6B	6B	2B	46...1500B	4B
Preamble	SFD	Destination Address	Source Address	Ether-type	Payload	FCS

- Avoids collisions on the network with cyclic polling mechanism
- Controlled Node (Slave) responds to Master Node controller
  - PollResponse as fast as possible after the reception of a PollRequest
  - Very often: Integrated 3 port hub or switch to allow line-topologies



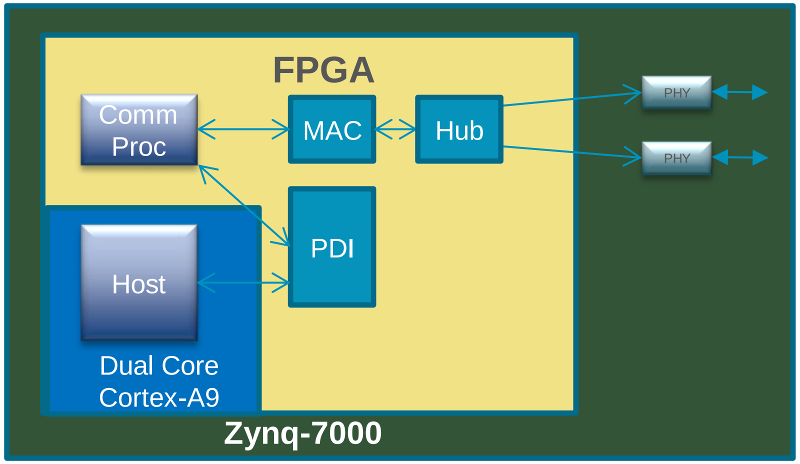
Performance Testing 2 Architectures

Architecture 1:
POWERLINK in **software** on Cortex-A9



- Use of ARM Core
  - Network runs in Cortex-A9
  - Standard Ethernet MAC is in use
  - Linux Ethernet drivers
  - Linux kernal 3.3

Architecture 2:
POWERLINK with **FPGA** Acceleration



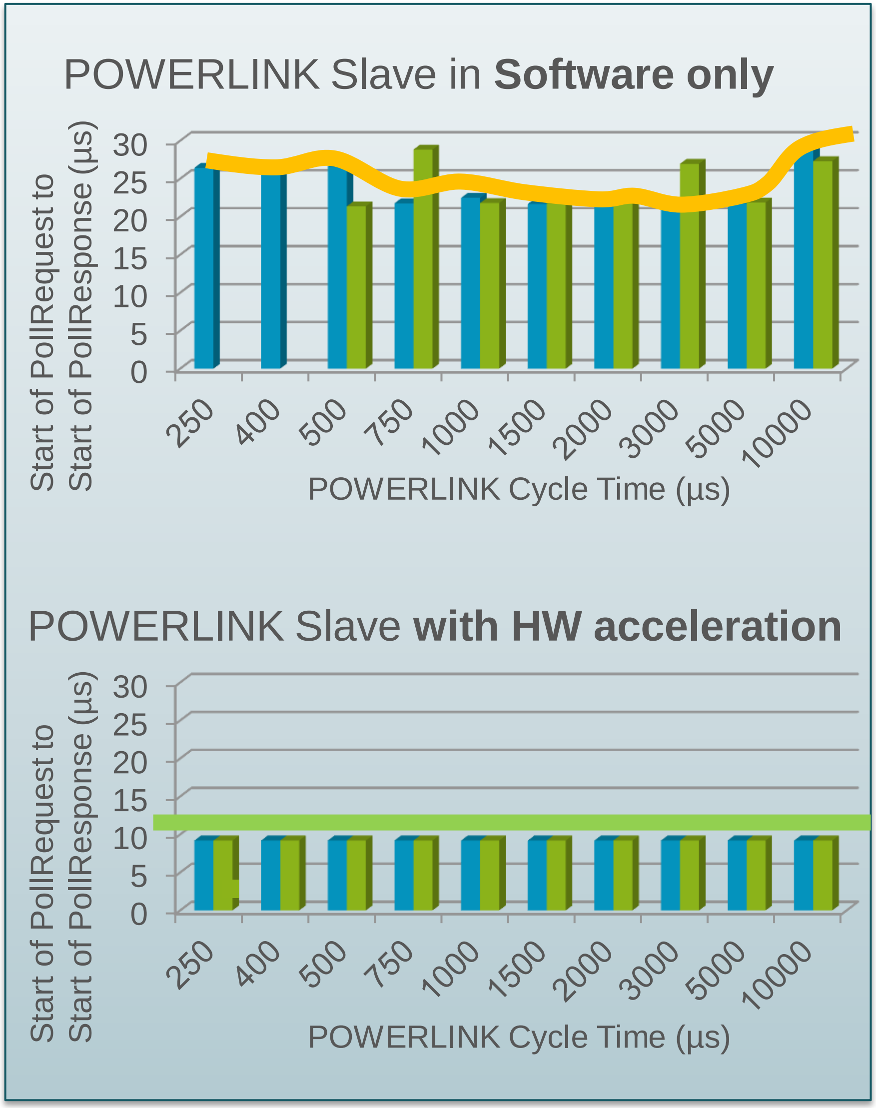
- Time critical functions are in FPGA:
  - Industrial Ethernet MAC
  - Process Data Interface (PDI)
  - Communication stack

In both options: The application is located in Cortex-A9

Highest Performance with HW Acceleration

Architecture 1

Architecture 2



Legend: no other Slaves 5 more Slaves

Findings

- Response time: 9 µs vs 20...30 µs
- Varying vs. constant response times
- Varying vs. constant minimum cycle times

Reasons

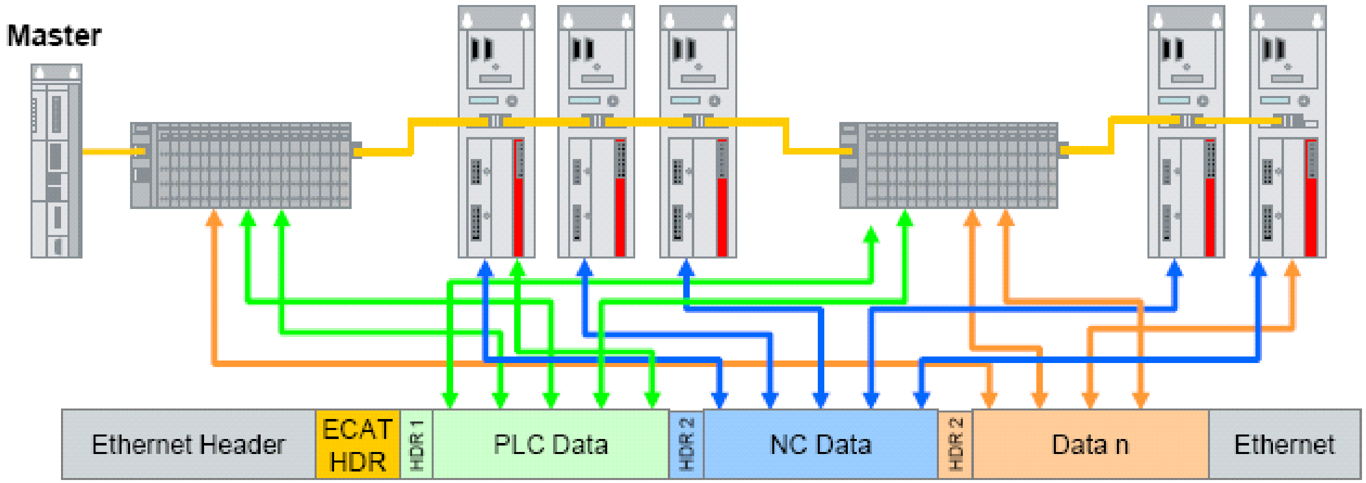
- Parallelization
- Least possible Inter Frame Gap with modified MAC in HW
- Less interrupts with filtering in HW
- Bare metal protocol implementation

Ethernet POWERLINK: Perfect accuracy with acceleration in HW

Case Study – EtherCAT on Zynq

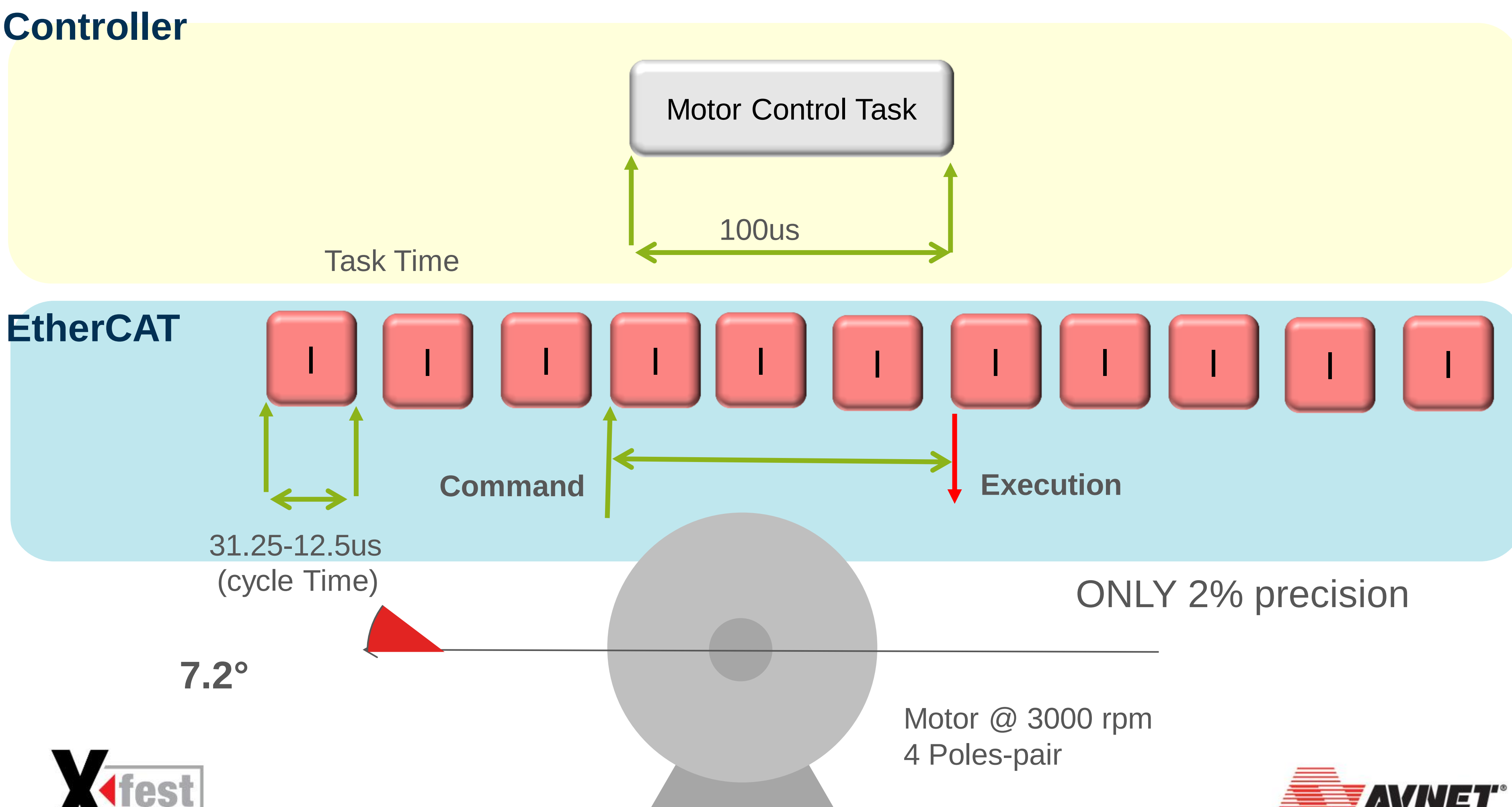
EtherCAT protocol

- **Use IEEE 802.3 Fast Ethernet**
  - Modified Layer 2-4
- **Process data is extracted and inserted “on the fly”**
  - EtherCAT Slave processes the frame in hardware
  - Frames are only delayed a few nanoseconds

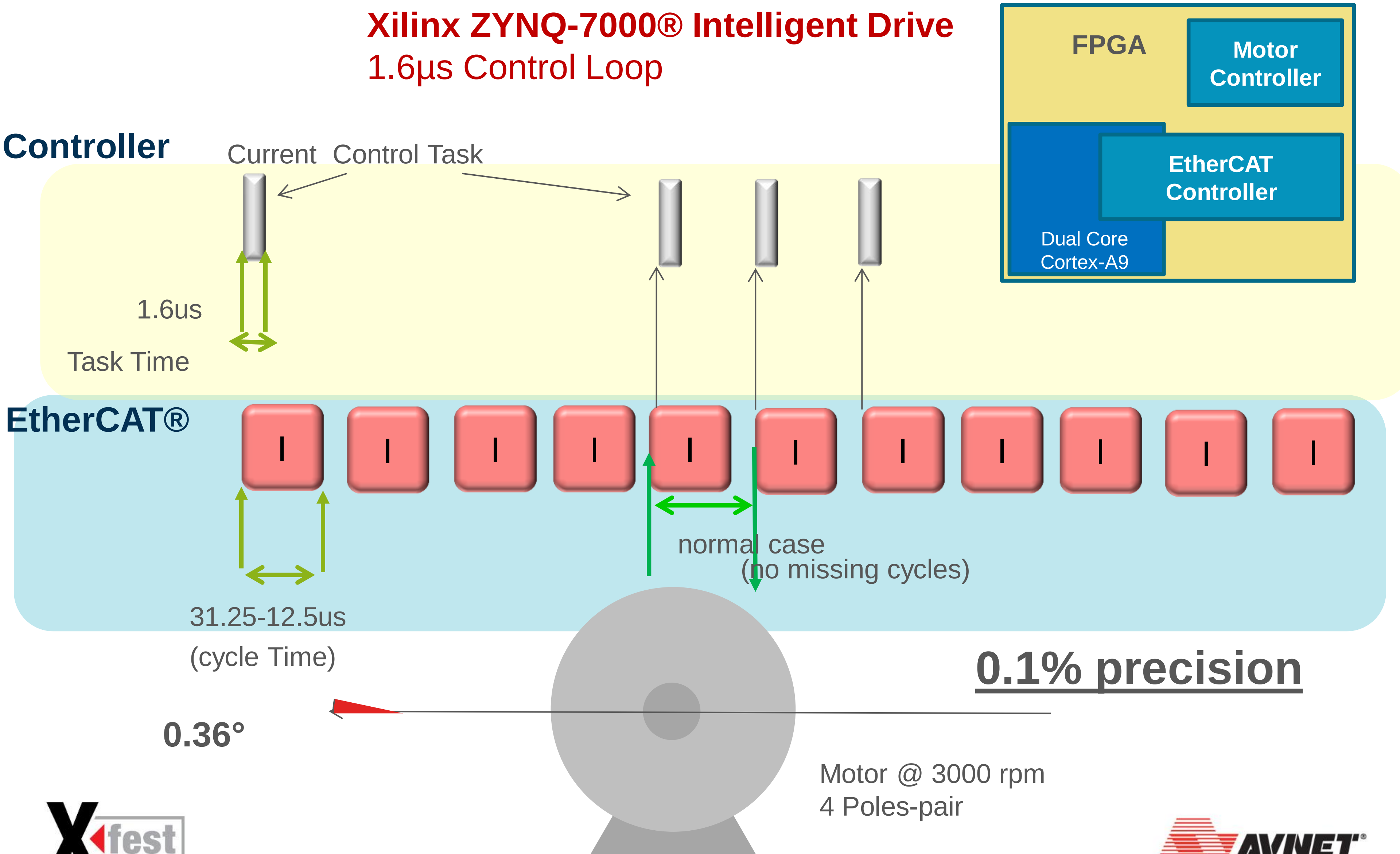


- **Asynchronous, event-triggered communication**

EtherCAT Performance is Often Wasted



EtherCAT on Zynq Increases Drive Precision



Smarter Industrial Connectivity

Forward Thinking Solution

Leading protocols – Leading partners – Flexibility

Xilinx Offerings

- Future proof
- Single chip integration
- Custom hardware functions
- Network acceleration
- Multi-network connectivity

VS.

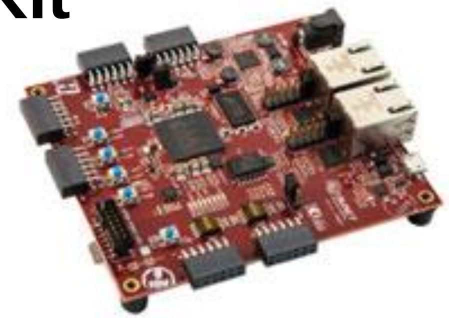
Industrial Ethernet ASICs

- Multi-chip system
- Software stack upgradable only
- No differentiation
- No support for evolution of protocols

Real-time Ethernet Development Platforms

- **Zynq / Analog Devices Intelligent Drives Kit**
  - Dual 10/100/1000 IEEE1588 PHYs
  - Third Ethernet port on ZedBoard
  - Full motor drive platform

- **Avnet’s Artix®-7 50T FPGA Evaluation Kit**
  - Dual 10/100 PHYs with IEEE1588 support
  - 256MB DDR3 memory
  - 6 Pmod™ interfaces (48 user I/O pins)
  - Controlled Node reference design (coming)



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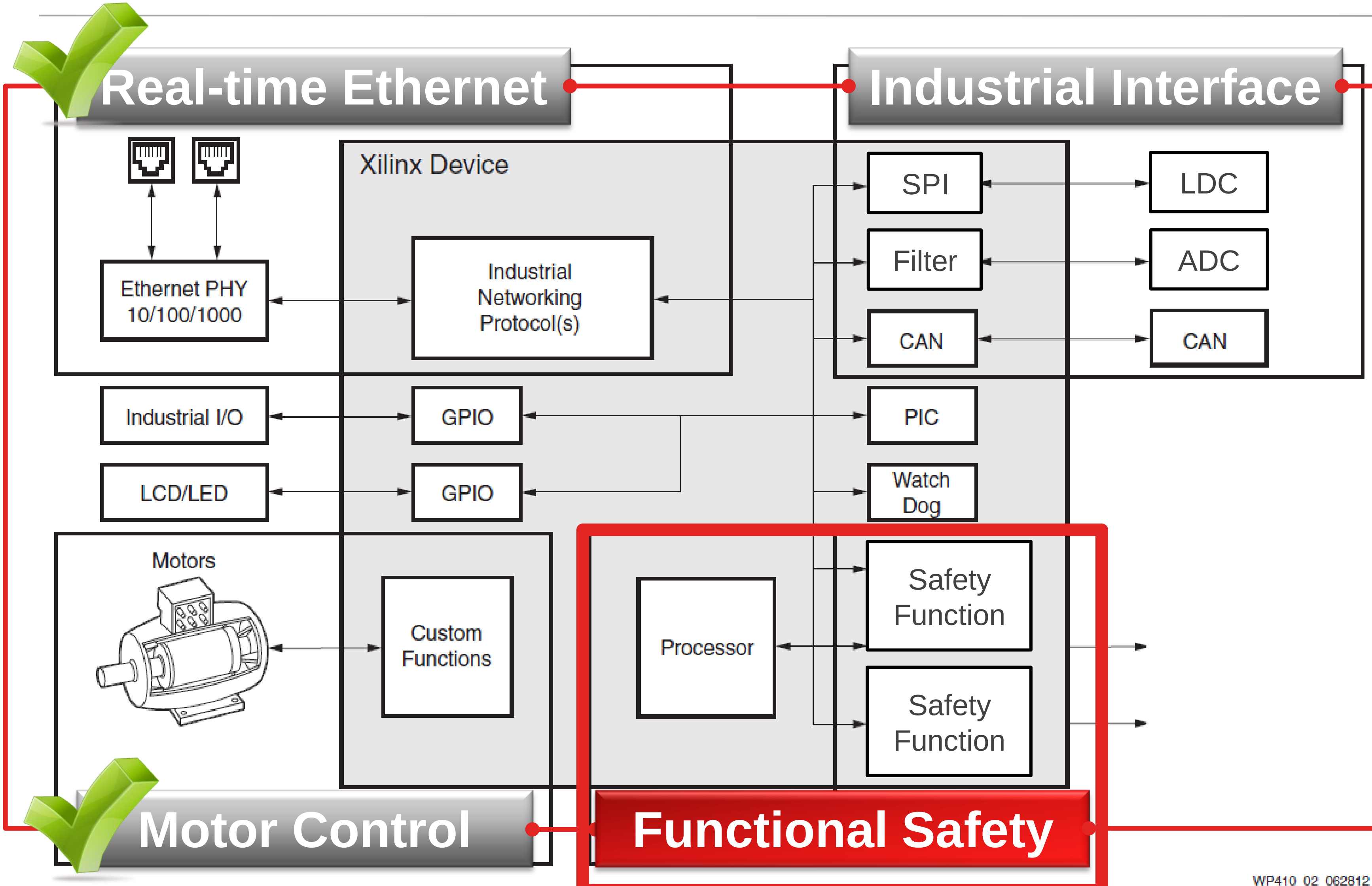

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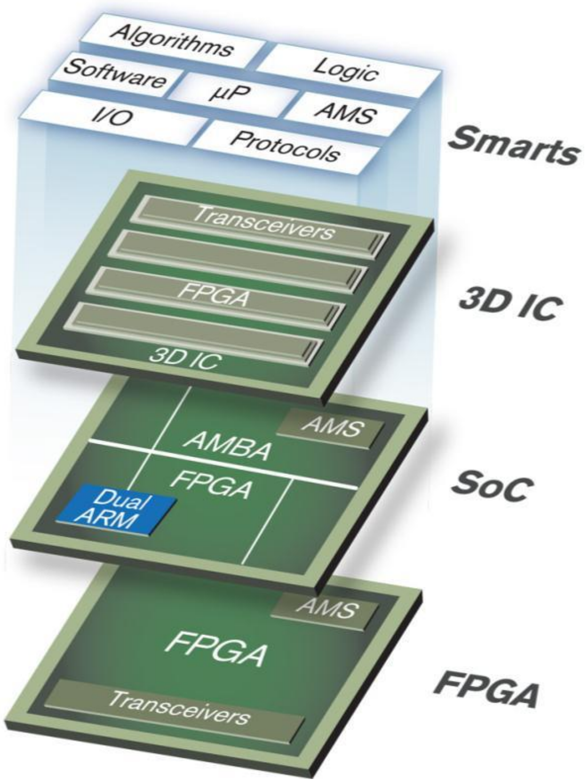
WP410_02_062812

IEC61508 Compliance

- "Functional Safety of Electrical / Electronic / Programmable Electronic Safety-related Systems"

- Annex E calls for: "Structures that isolate and decouple physical locations"

- Can this be accomplished in a System on Chip (SoC)?



Xilinx Solves Functional Safety Challenges

- Two-stage design flow to ensure functional separation
  - Isolation Design Flow (IDF)
  - Isolation Verification Tool (IVT)
- Approved by TÜV-SÜD

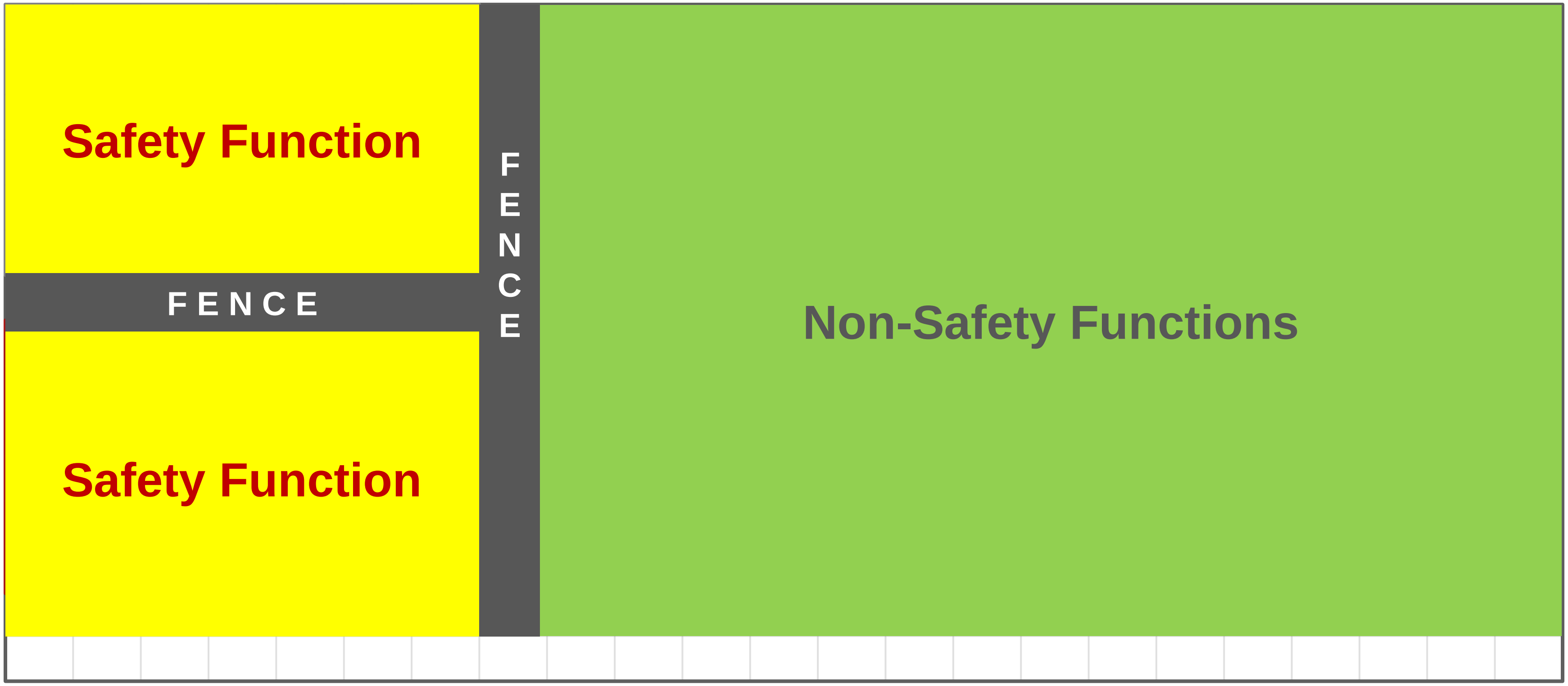
IEC 61508	SIL1 to SIL3
ISO 26262	ASIL-A to ASIL-D

- Uses the ISE Design Suite 14.7 (PlanAhead floorplanner)

ISOLATION AND TRUSTED ROUTING

Case	Random Failure	Systematic Failure	Diagnostic Coverage	SIL 3	IEC 61508-7 (clause)
SEU	Mitigated	-	High	R	A.3, A.7, A.8
Complete hardware redundancy	Mitigated	-	High	R	A.7.3
Diverse hardware	Mitigated	Mitigated	High	R	A.7.3 & B.1.4
Information redundancy	Mitigated	-	High	R	A.7.6
Code protection	Mitigated	Mitigated	High	M	A.6.2
Increase of interference immunity	Mitigated	Mitigated	High	M	A.11.3

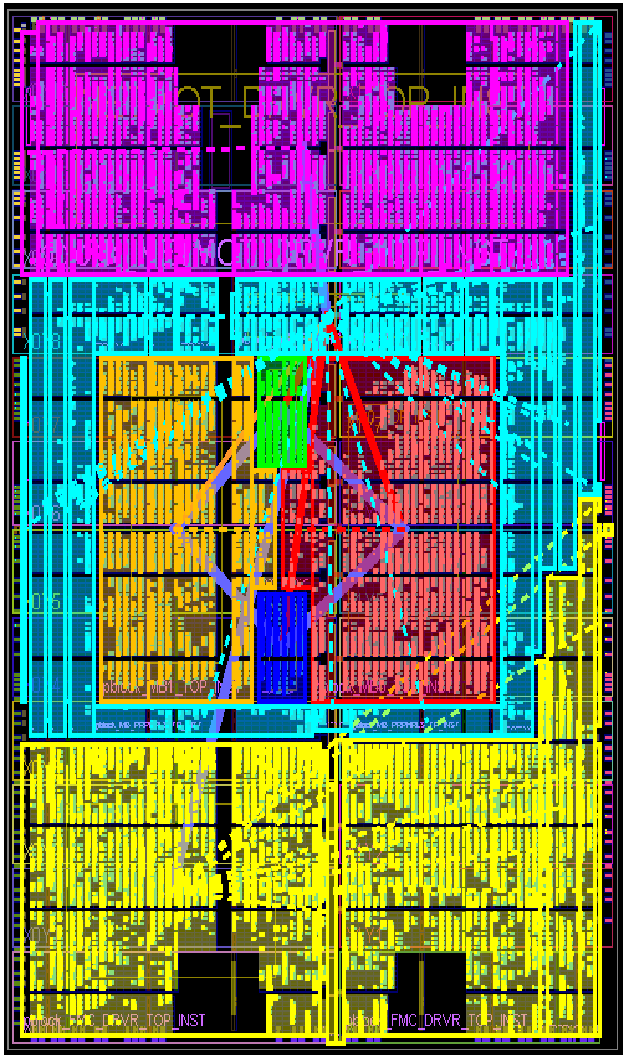
Isolation Design - Basic Concept



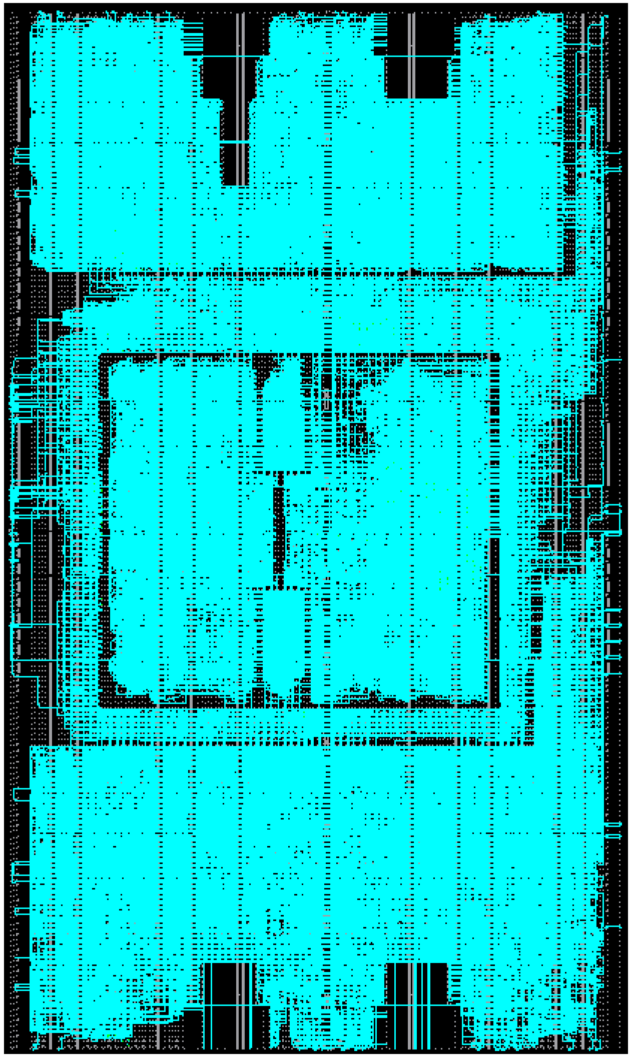
- IDF methodology creates physically isolated modules
- IVT software ensures elimination of single points of failure

Isolated Design in PlanAhead and FPGA Editor

PlanAhead

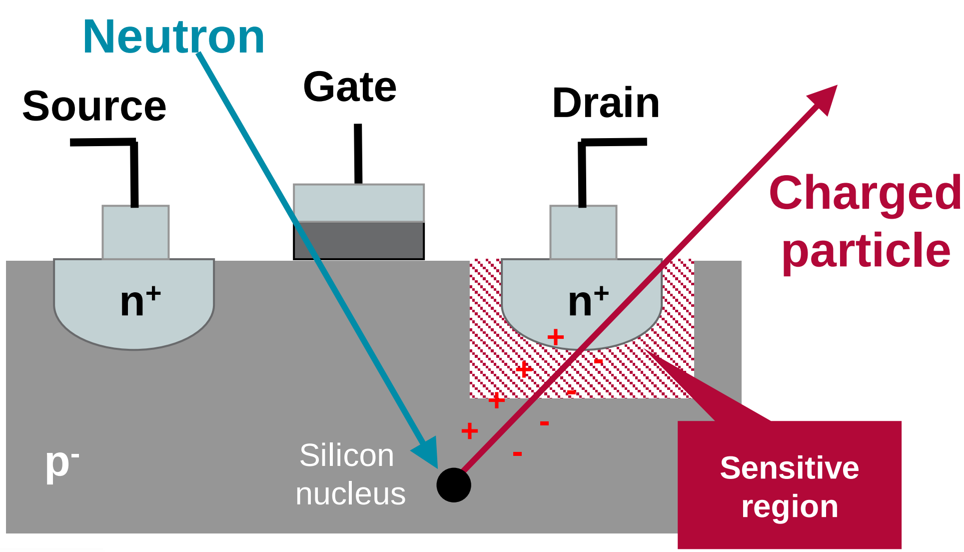


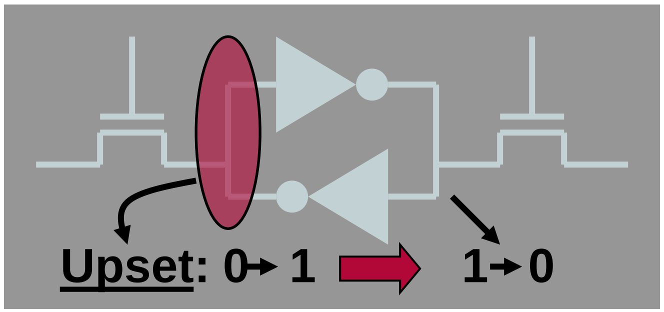
FPGA Editor



Recurring question: Soft Error Effect

- **SEE = soft error effect**
  - SEU = soft error upset, a bit flips 0->1, 1->0
  - SET = single event transient, 1->0, 0->1 for a few hundred ps
  - MBU = multiple bit upset (smaller geometry = more bits hit)
  - Latch-up = destruction due short circuit from charged particle





SRAM Cell

Xilinx Has Lowest Soft Error Rate + Built In Mitigation

- Integrated Configuration RAM CRC and ECC
  - Runs in background
  - Scans most devices in < 20-30ms
  - Correct flips & continue running without reconfiguration!
  - Corrects bit flip very quickly (< 1msec)
  - Zero impact on design performance

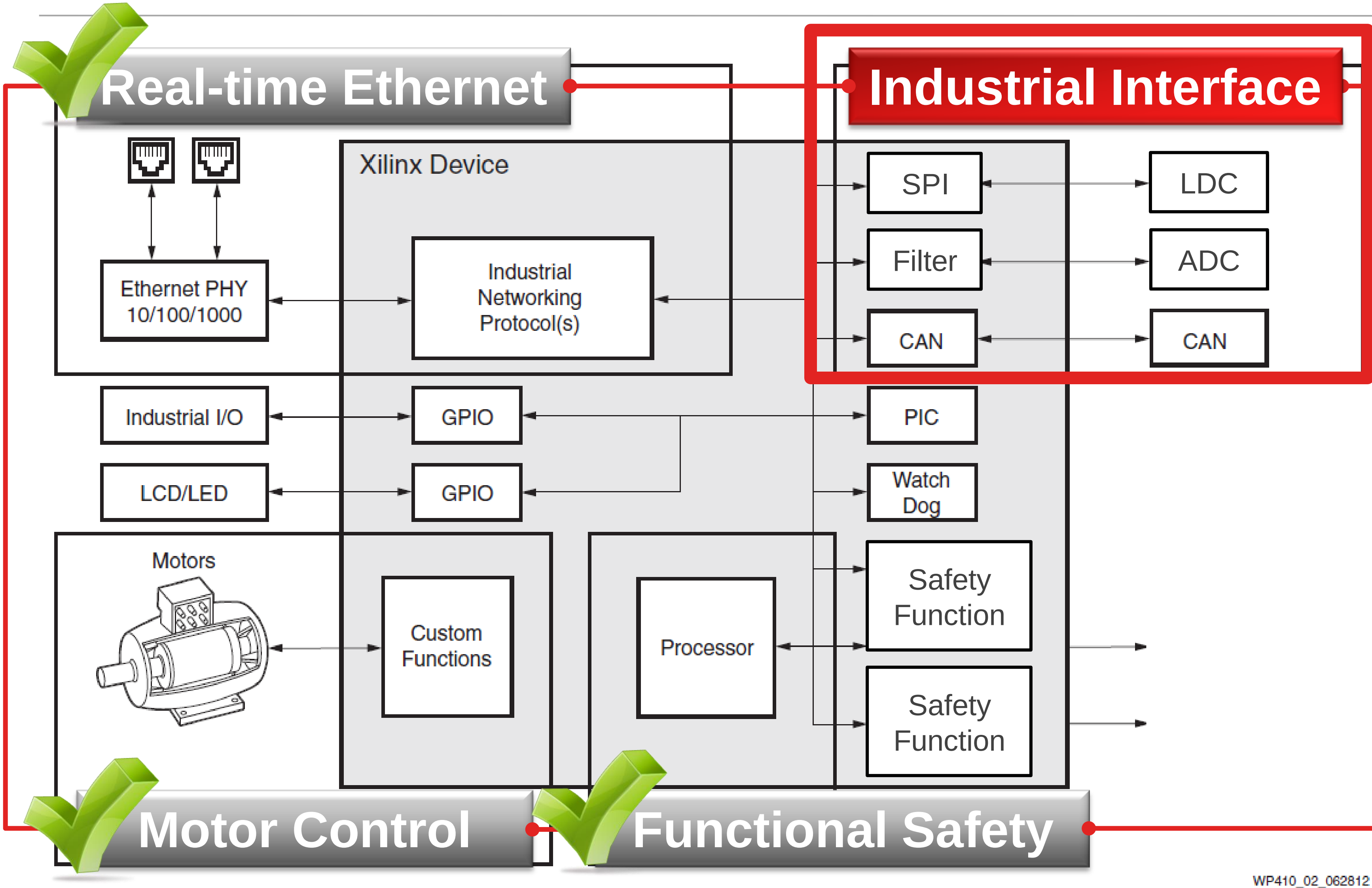
- Soft Error Mitigation (SEM) IP core
  - Error classification
  - Automatically detects, classifies, and corrects SEU and MBU

Xilinx Functional Safety References

www.xilinx.com/applications/isolation-design-flow

- **Xilinx Functional Safety Package** – ask your local Avnet FAE
- XAPP1086 – Developing Secure and Reliable Single FPGA Designs With Xilinx 7 Series FPGAs using Isolation Design Flow
- WP412 – The Xilinx Isolation Design Flow for Fault-Tolerant Systems

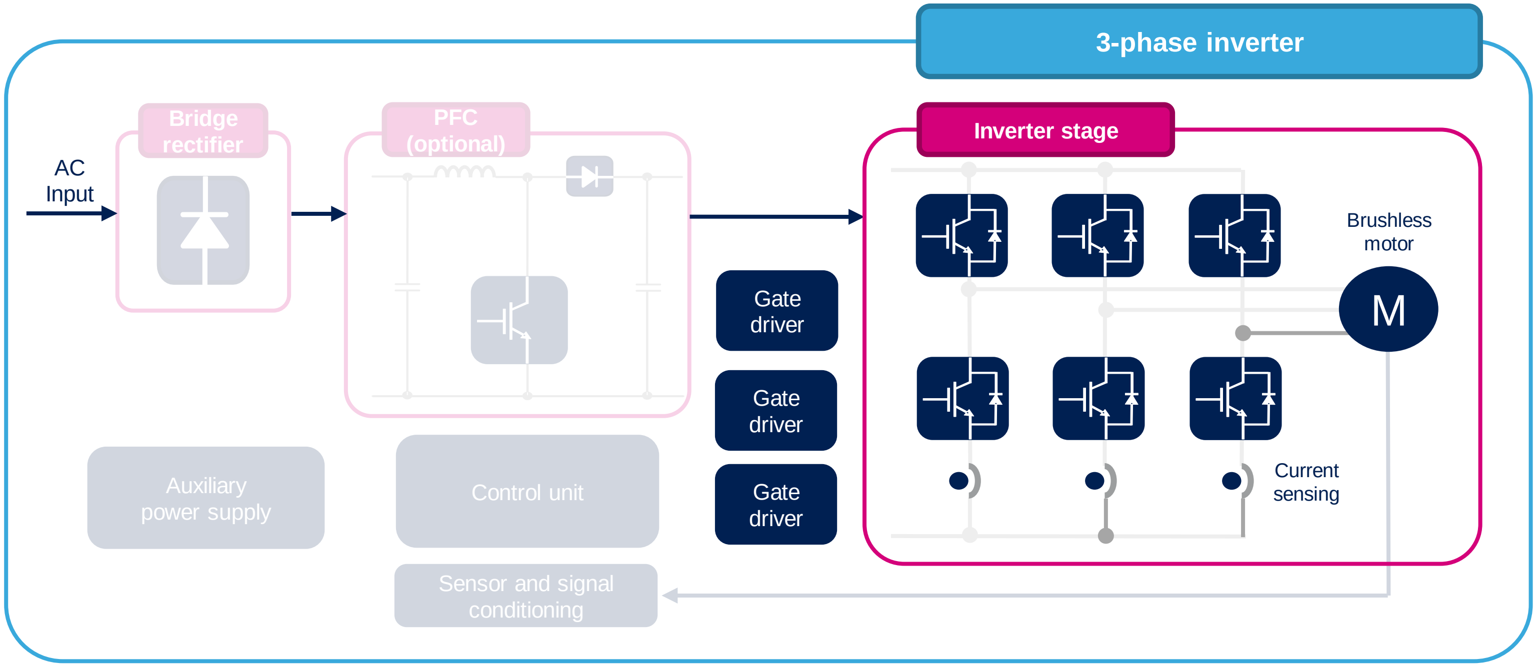
Agenda



Real-time Ethernet
Industrial Interface
Xilinx Device
Ethernet PHY 10/100/1000
Industrial Networking Protocol(s)
SPI
Filter
CAN
LDC
ADC
CAN
Industrial I/O
GPIO
PIC
LCD/LED
GPIO
Watch Dog
Motors
Custom Functions
Processor
Safety Function
Safety Function
Motor Control
Functional Safety
WP410_02_062812

Simpler Power Stages

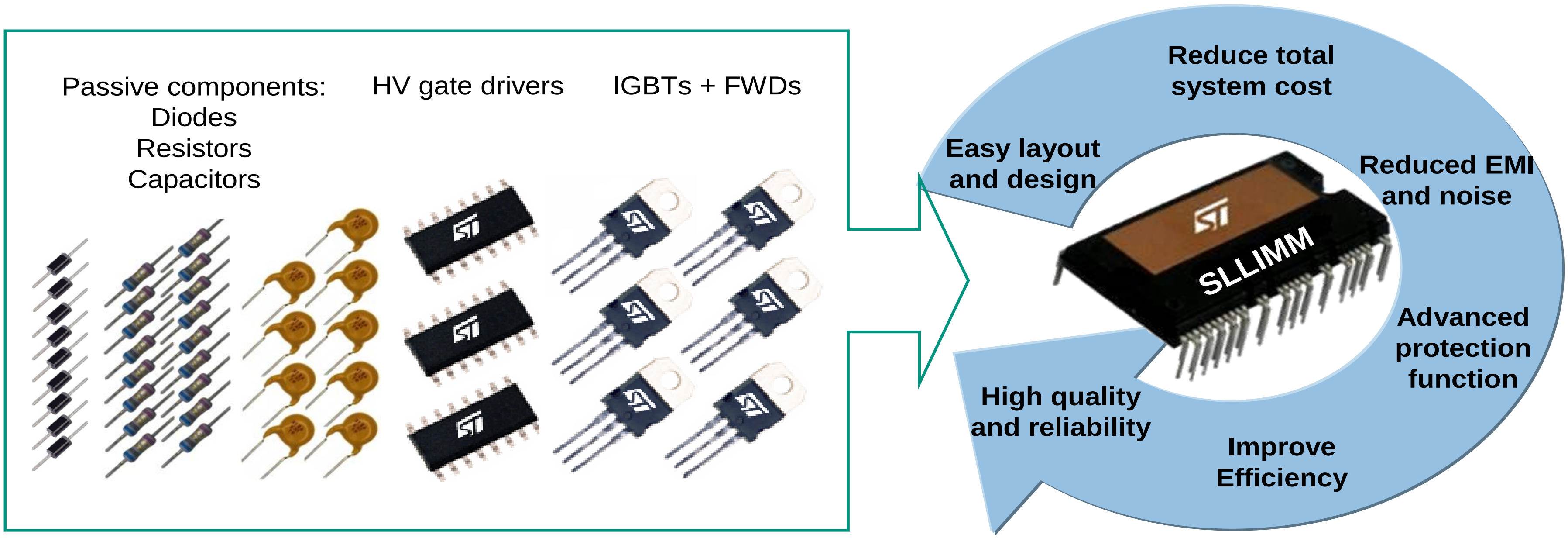
3- Phase Inverter Stage – Discrete or Module



- **IGBT**: 600V,10 to 30A, Trench gate fieldstop — STGxxH60DF
- **IGBT**: 1200V 15 to 40A Trench gate fieldstop — STGxxH120DF2
- **smartDRIVE™ Gate Driver**: 600V, Half Bridge gate drivers — L639x series
- **SLLIMM™ Inteligent Power Modules** — Xfest Product Spotlight — STGIPxxC60(-H) STGIPNxxC60(-H)

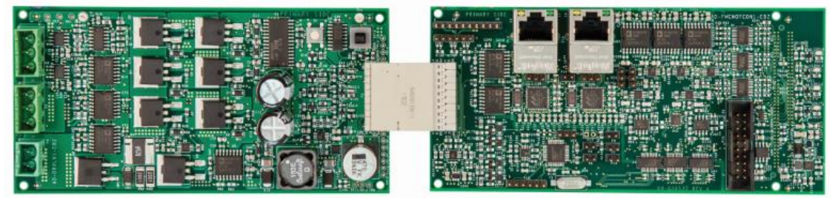
Why SLLIMM™ for motor control?

Integration of more than 30 discrete components

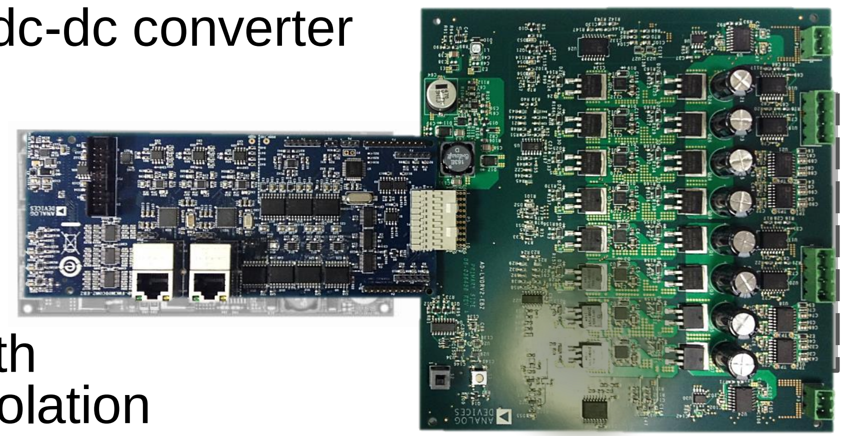


Robust Signal Chains

Analog Devices Isolated Precision Signal Chain



- **AD-FMCMOTCON1-EBZ**
  - AD7401A isolated SigmaDelta modulators
  - ADuM7640/1 *iCoupler*® six-channel digital isolators
  - ADuM5000 *isoPower*® isolated dc-dc converter



- **AD-FMCMOTCON2-EBZ**
  - Isolated drive of 2 motors
  - AD7403 isolated SigmaDelta with improved SINAD, ENOB, and isolation
  - ADuM7223 isolated gate driver up 1MHz switching
- Polyphase filter banks implemented in the Zynq PL increase system sampling rate up to 10Msps and reduce latency

MAX14890 - Maxim Incremental Encoder Receiver
Robust Quad RS-422/TTL/HTL Receiver + 2 Digital Inputs

Features

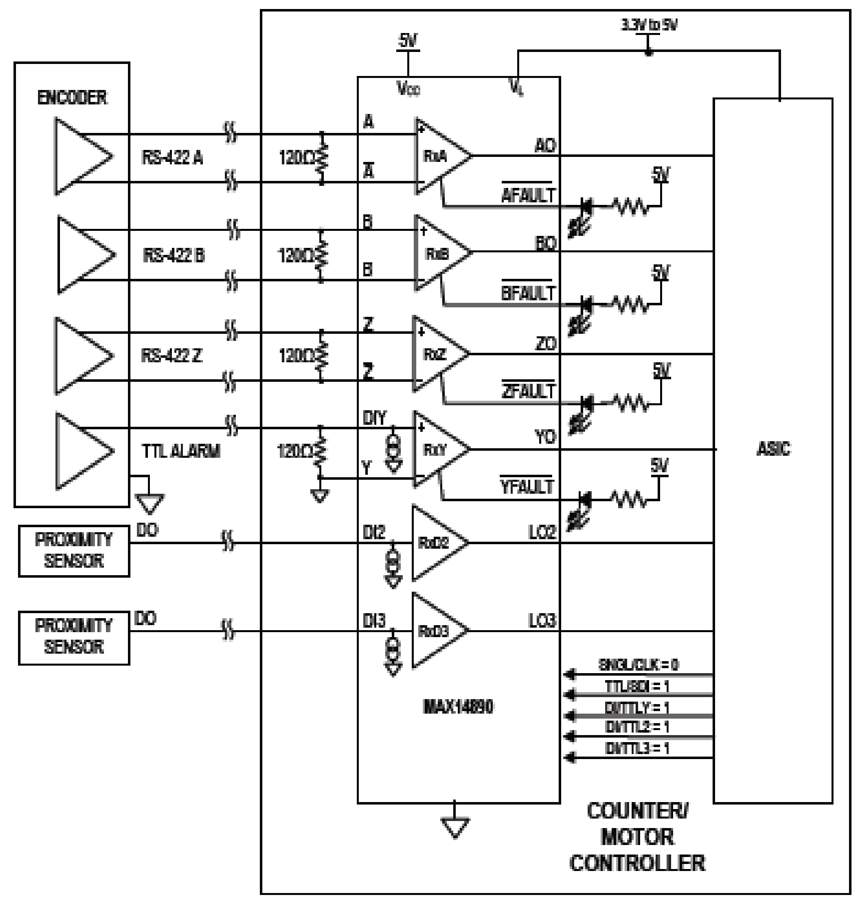
- ±40V Fault Protection
- Fault Det. (Open, Short, OV)
- ±27V CMR Range
- 4 RS-422/TTL/HTL Receivers
- 2 DI/TTL Receivers

Benefits

- Integrated Robustness increases uptime and eliminates circuitry
- Eliminates 2 external DI
- Reduces SKU's with flexible RS-422, TTL, HTL encoder interfaces

Applications

- Motion controller
- Encoder Interface
- Pulse Counter Module
- Servo Controller Commutator



ENCODER CIRCUIT WITH RS-422 SIGNALS AND TTL ALARM SIGNAL

In Design (Samples Available)

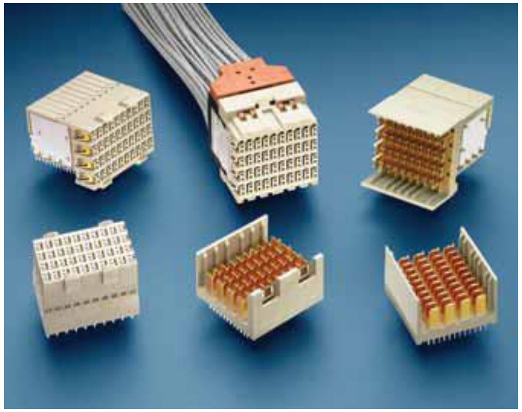
Xfest

maxim integrated™ AVNET®

TE Connectivity Industrial RJ45 Connectors

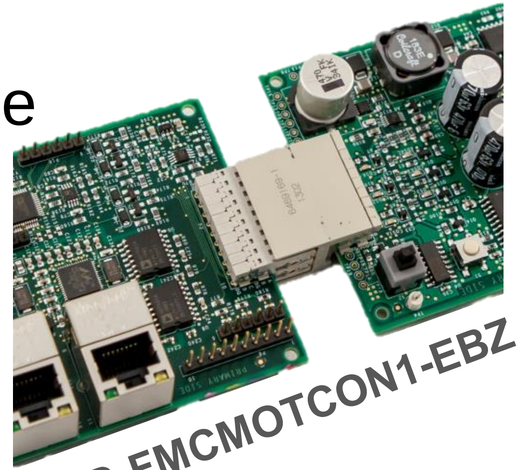
- TE Industrial Ethernet RJ-45 connectors utilize a “common core” design for enhanced flexibility
  - Interchangeable with plastic or metal housings or receptacles
- Additional features include:
  - Fast termination technology
  - Field installable
  - Data rates of 100 Mbit/s (4 pos.) or 1Gbit/s (8pos.)
  - Rugged locks
  - High reliability

TE Connectivity HM-Zd PCB Mount Connectors



- Up to 12.5 Gb/s performance
- Density up to 16 differential pairs/cm
- Available in 2, 3 and 4 pairs/column
- Designed specifically for high speed differential applications
- Vertical press fit pin headers and right angle press fit receptacles
- Unobstructed routing channels on both daughtercard and backplane

Product Spotlight



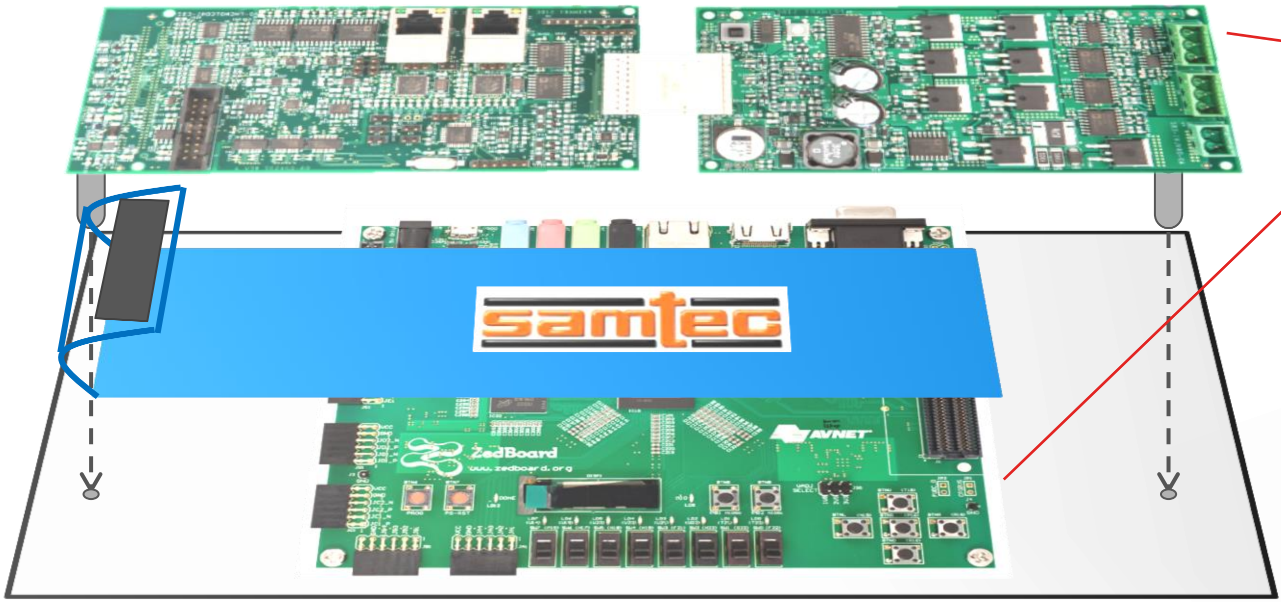
AD-FMCMOTCON1-EBZ

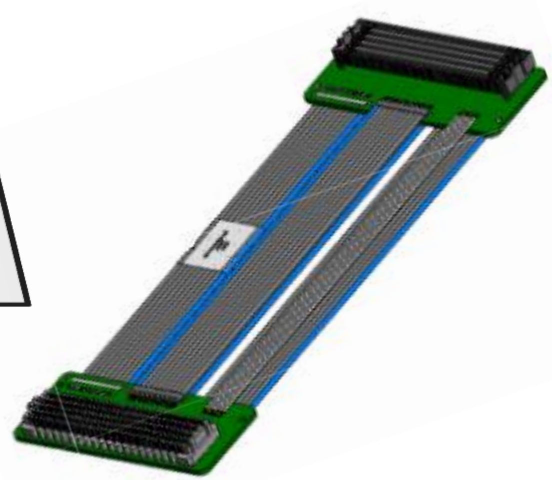
TE connectivity Authorized Distributor

VITA 57 (FMC) SEARAY™ Cable Assemblies

Zynq / ADI Intelligent Drives Demo

Xfest Product Spotlight





- Samtec FMC 300mm SEAM to SEAF connectors
- Flexible cable assembly
- Enables custom system footprint

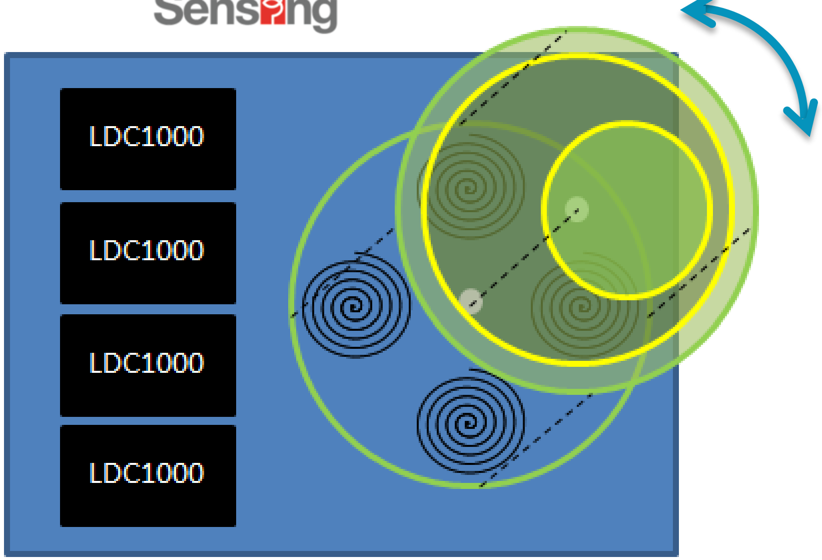
Samtec's FMC Cable Assembly
HDR-169472-01
www.em.avnet.com/samtecfmc

Position Sensing

Inductive Sensing for Motor Position Encoding

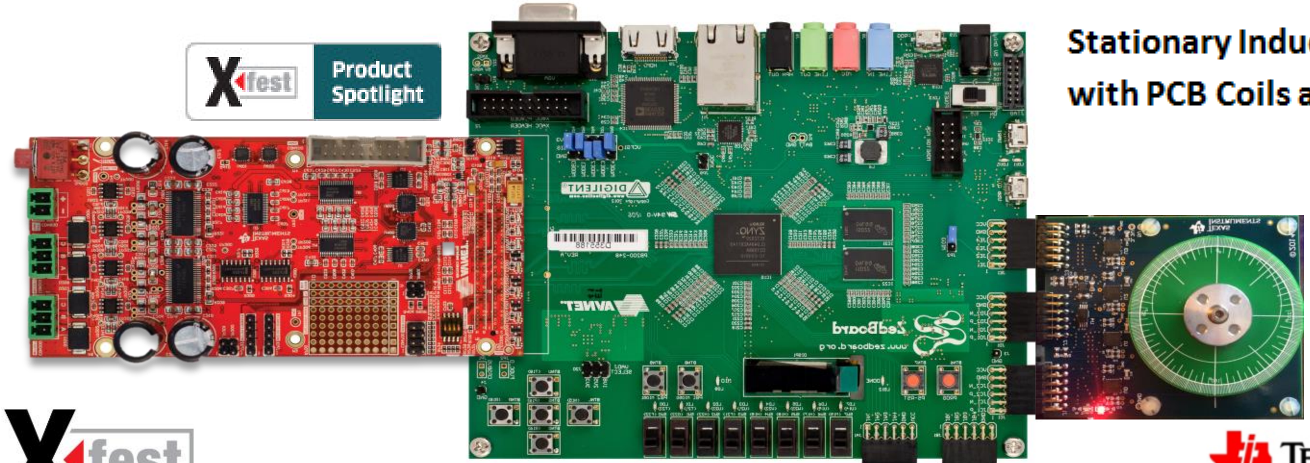
- The LDC1000 senses the absolute position and direction of the motor's rotor by measuring the unique inductance waveform generated by a rotating conductive target.

Rotating Target



Stationary Inductive Sensing Board with PCB Coils and LDC1000s

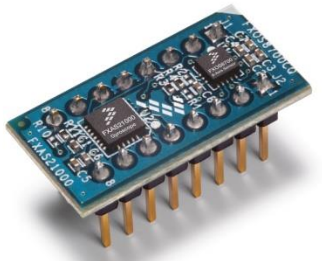
Product Spotlight



Xtrinsic Accelerometer, Magnetometer & Gyro

FXOS8700CQ 3D Accelermoter & 3D Magnetometer

- 1.95V to 3.6V supply voltage, I/O 1.6V – 3.6V
- Lowest noise gcell and mcell
- Fast system response and power savings
- 32 sample FIFO with burst read



DIP95000-9AXIS-H

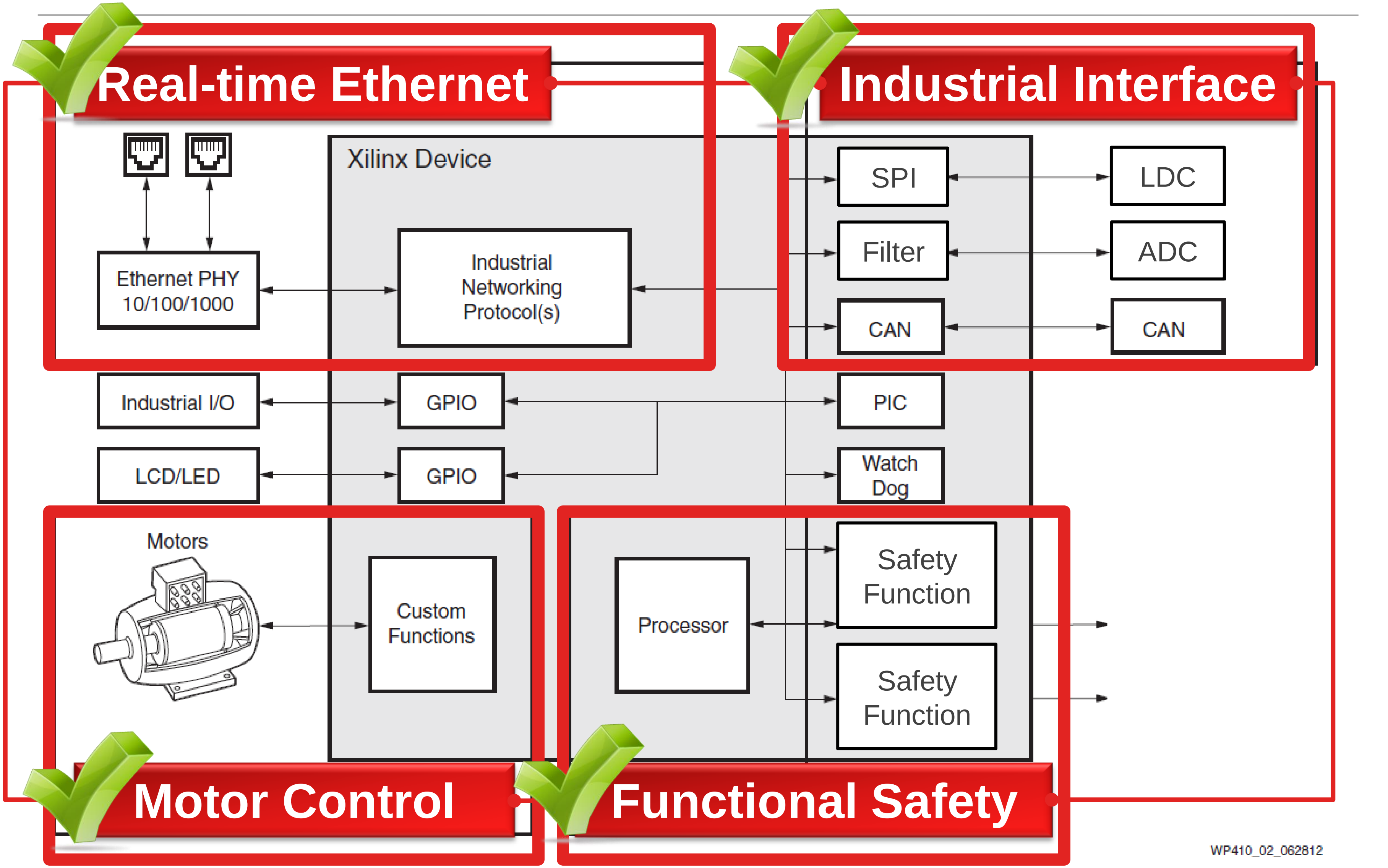
IncludesFXOS8700CQ & FXAS21000

Available Q4'13

FXAS21002 3-Axis Digital Gyroscope

- Lowes power 3.0mA (Active), 2uA (Standby)
- ISF support for 9Axis solutions
- 1.95-3.6V supply voltage
- Output data rates (ODR) from 1.5625 Hz to 200Hz
- Selectable Full Scale ranges +/-200, +/-400, +/-800, +/-1600
- Angular Random Walk: 0.055 dps/rt(Hz).
- Angular Velocity acceleration resolution <0.2°/s
- Programmable interrupts
- Power saving features

Agenda


Real-time Ethernet
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Ethernet PHY 10/100/1000
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SPI
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CAN
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GPIO
PIC
LCD/LED
GPIO
Watch Dog
Motors
Custom Functions
Processor
Safety Function
Safety Function
Motor Control
Functional Safety
WP410_02_062812

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Q&A forums for each course

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Kiitos
Maake
Asante
Shukria
Dhanyavadagalu
감사합니다
Dankscheen
спасибо
Kam Sah Hammida
اركشت
Manana
Dankon
Matondo
Dank Je
Mauruuru
Biyan
Diolch i Chi
Terima Kasih
Taiku
Blagodaram
Tack
Chokrane
Ngiyabonga
Dziekuje
Grazie
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cảm ơn bạn
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Mèsi
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ありがとう
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Nuwun
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Rahmat
Di Ou
Welalin
Djiere Dieuf
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Merci
Go Raibh Maith Agat
Eskerrik Asko
Salamat
ขอบคุณ
Najis Tuke

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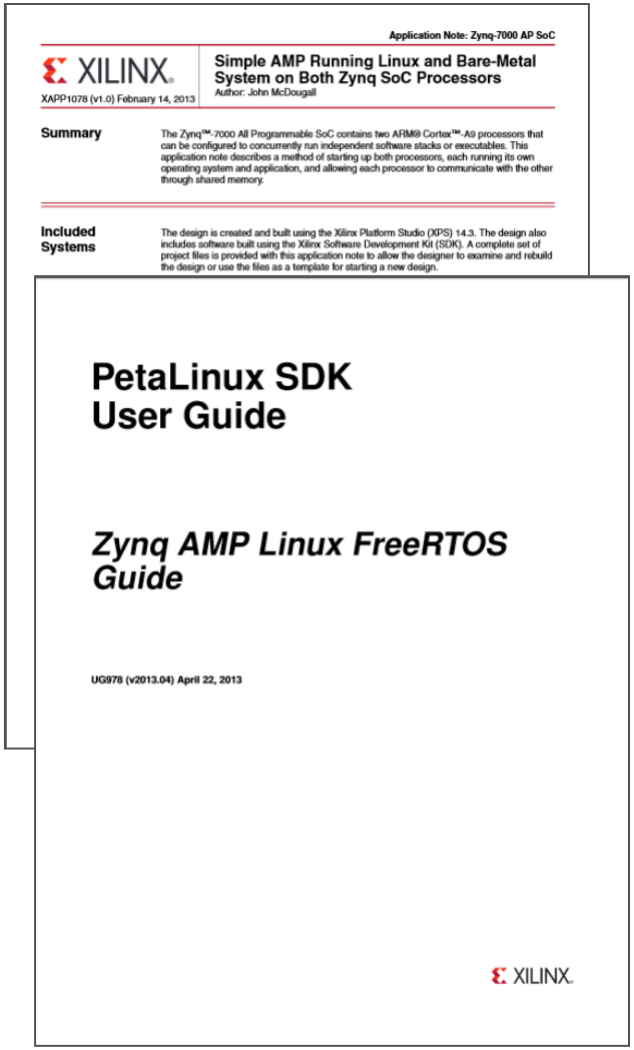
AVNET

Appendix

Zynq-7000: Multi-OS Options

- Different approaches meet different requirements
- XAPP1078: Simple AMP Running Linux and Bare-Metal System on Both Zynq SoC Processors
- XAPP1079: Simple AMP Bare-Metal System Running on Both Cortex-A9 Processors
- UG978: Zynq AMP Linux FreeRTOS Guide
- 3rd party Hypervisor and TrustZone®


Application Note: Zynq-7000 AP SoC

XILINX.

XAPP1078 (v1.0) February 14, 2013

Simple AMP Running Linux and Bare-Metal System on Both Zynq SoC Processors

Author: John McDougall

Summary The Zynq™-7000 All Programmable SoC contains two ARM® Cortex™-A9 processors that can be configured to concurrently run independent software stacks or executables. This application note describes a method of starting up both processors, each running its own operating system and application, and allowing each processor to communicate with the other through shared memory.

Included Systems The design is created and built using the Xilinx Platform Studio (XPS) 14.3. The design also includes software built using the Xilinx Software Development Kit (SDK). A complete set of project files is provided with this application note to allow the designer to examine and rebuild the design or use the files as a template for starting a new design.

PetaLinux SDK User Guide

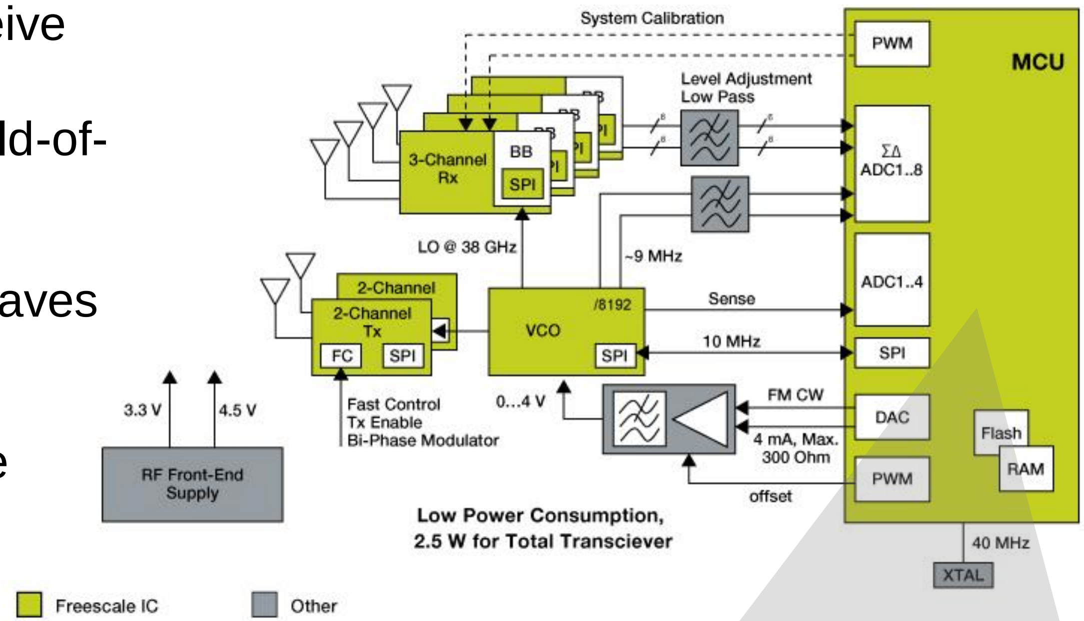
Zynq AMP Linux FreeRTOS Guide

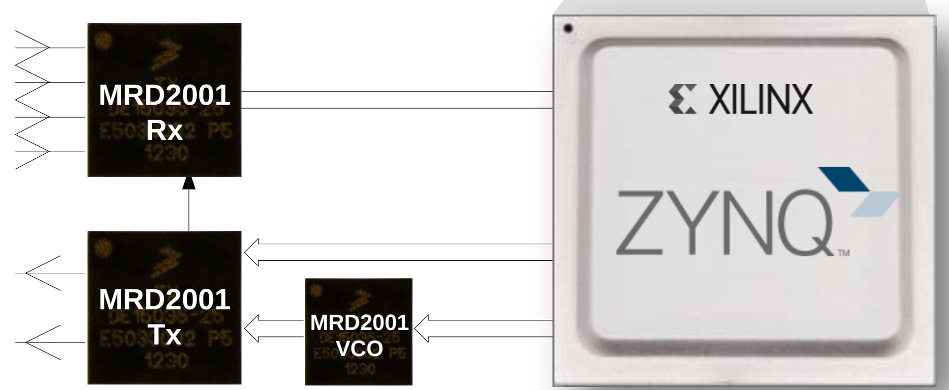
UG978 (v2013.04) April 22, 2013

XILINX.

MRD2001 77GHz Front-end Radar Chipset

- Scalable to 4 transmit, 12 receive
- Beam steering across wide field-of-view
- Integrated BB filter and VGA saves on the total bill of materials
- Best phase noise performance
  - -85 dBc/Hz at 100 kHz offset
  - -95 dBc/Hz at 1 MHz offset
- Low 2.5W power consumption
- Applications
  - Automotive ADAS
  - Industrial safety
  - Security intrusion detection
  - Robotic vision

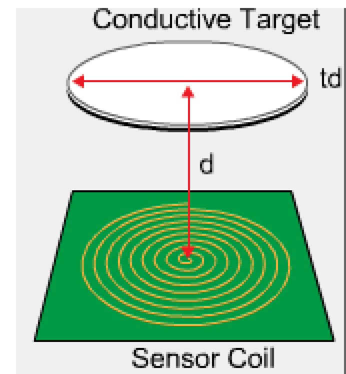




Texas Instruments Inductive Sensing

- LDC1000 – industry's first inductance-to-digital converter

- Use the inductive properties of coils, springs, and other devices to form sensors that deliver higher resolution, better reliability, and greater flexibility than other sensing solutions



- Micron resolution