PRESENTED BY

Bryan Fletcher

UltraScale™ Memory Interfaces

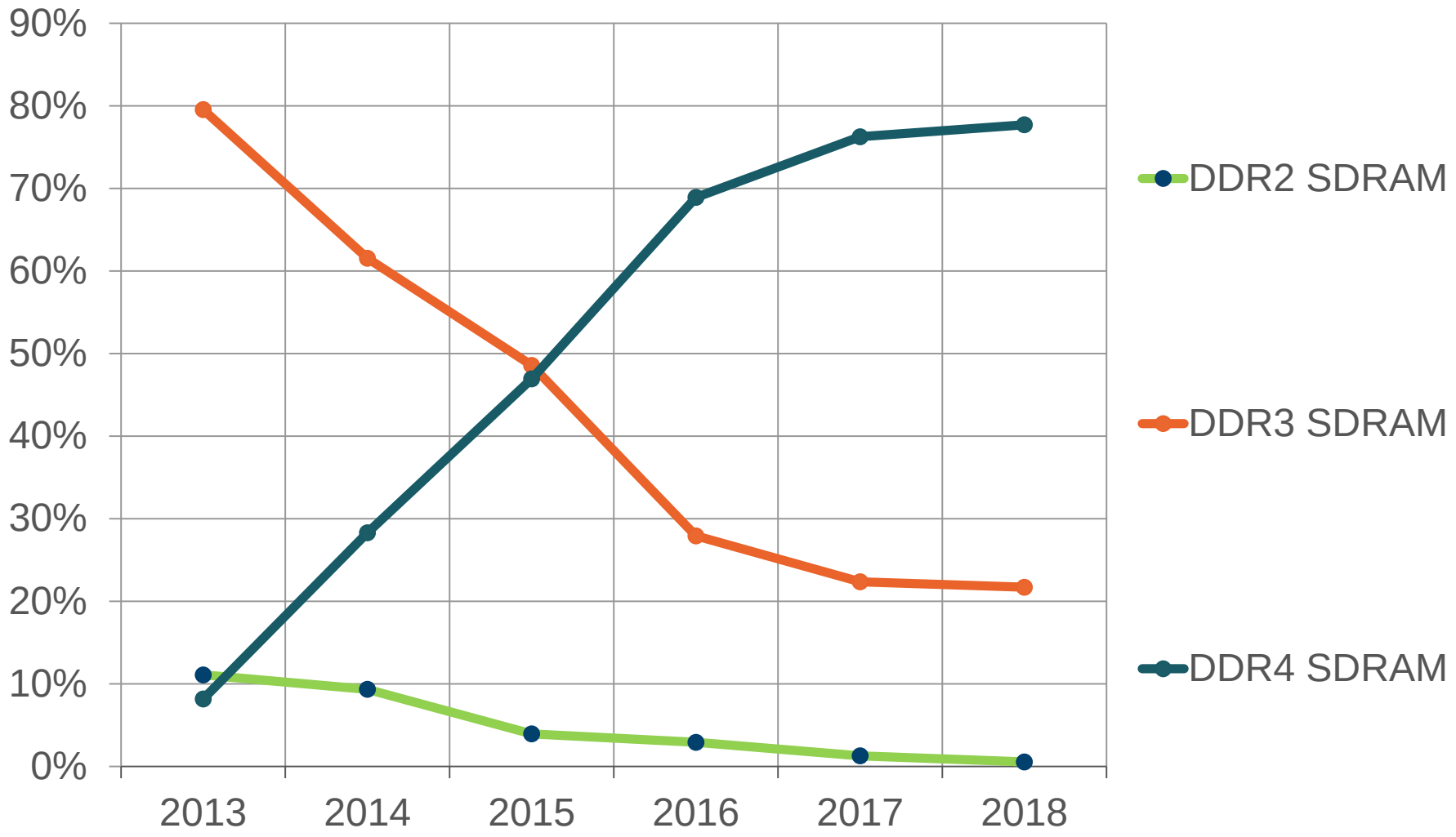
Accelerating Your Success™

Memory Interface Criteria

- **System designers prefer memory interfaces with**
  - Less **P**ower
  - More **P**erformance
  - Lowest **P**rice per bit

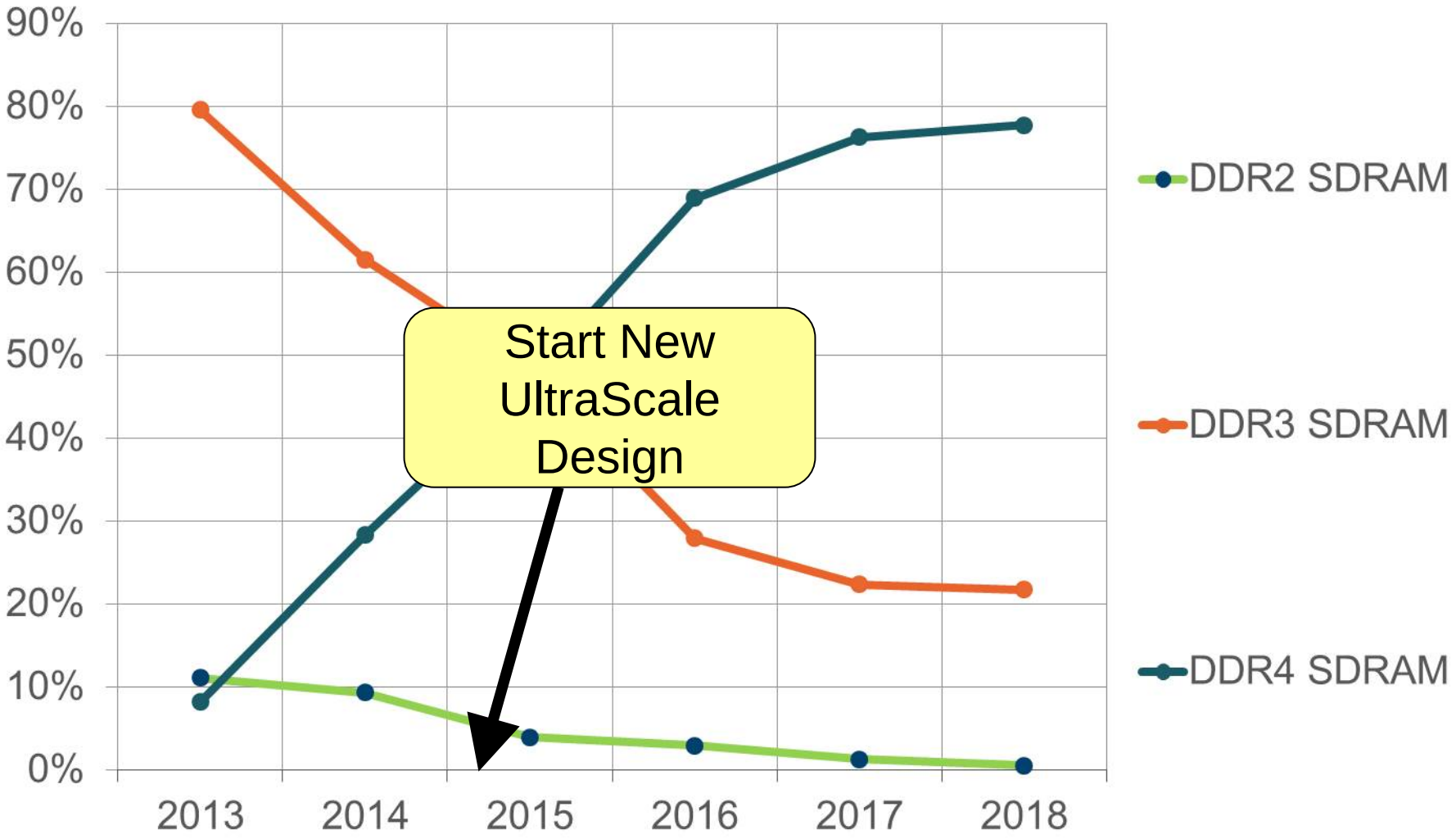
- **DDR4 delivers in all three areas with UltraScale™ (compared to DDR3)**

DDR SDRAM Market Share



Source: Gartner (March 2014)

Design Timeline



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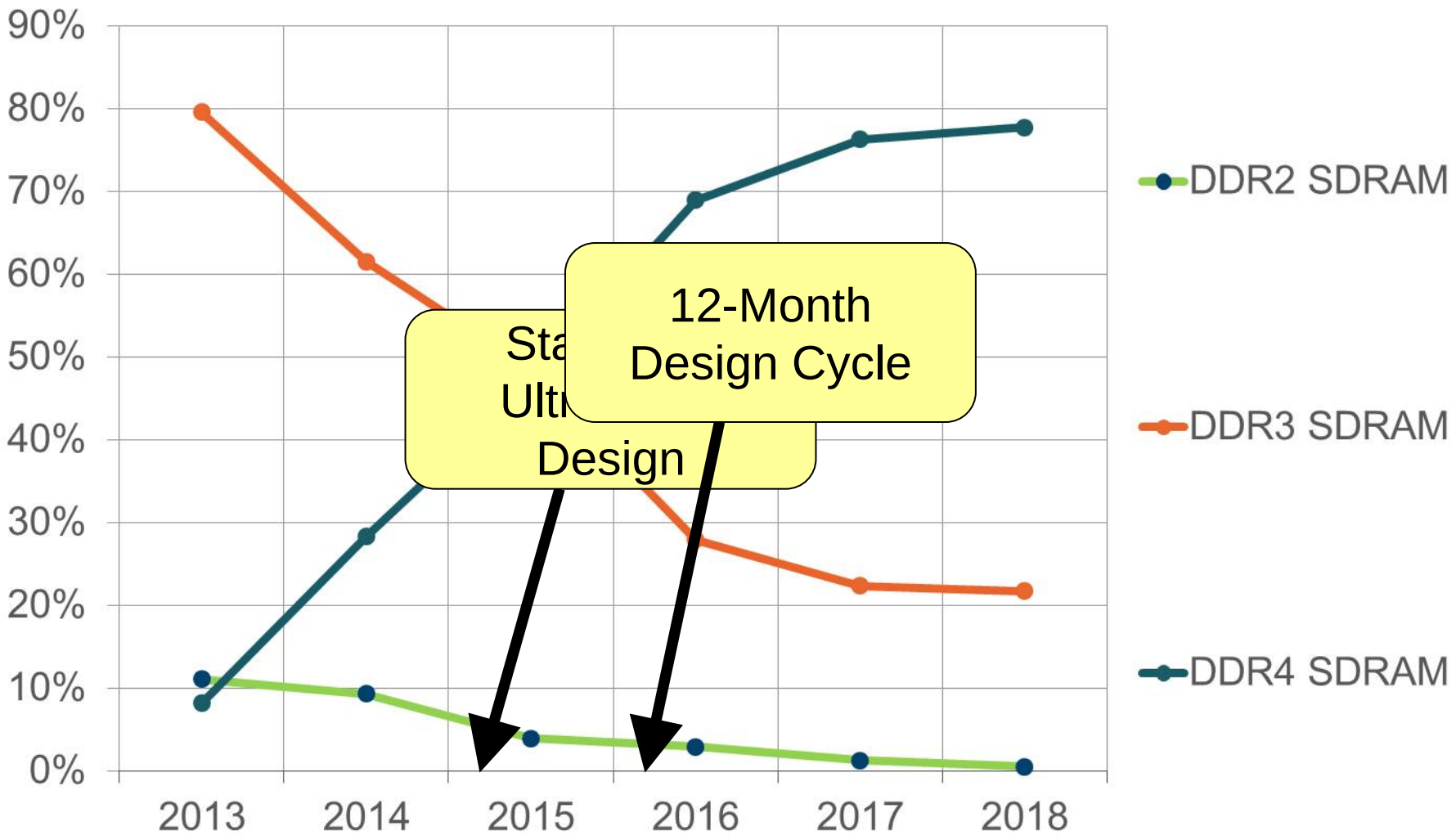

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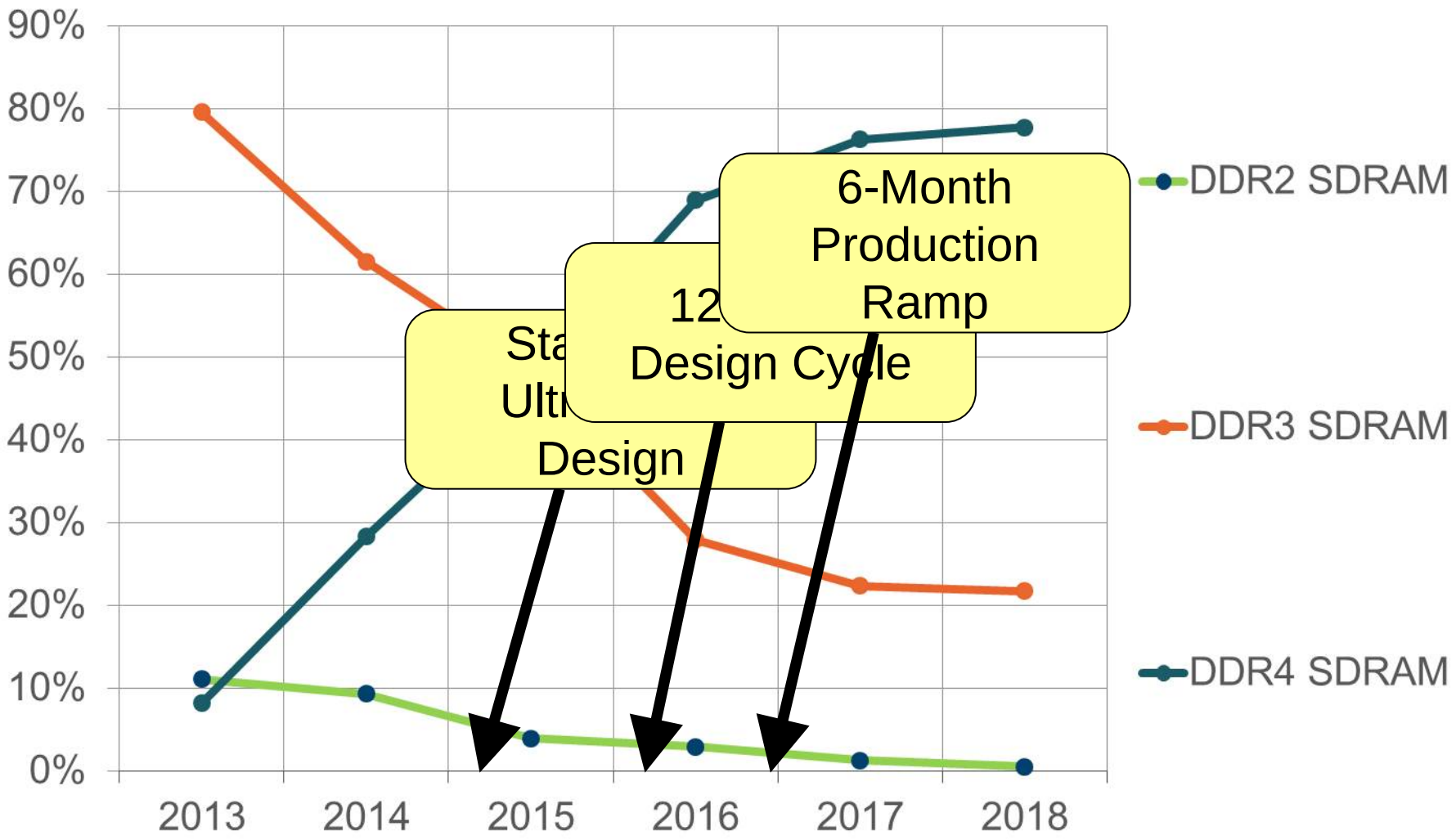

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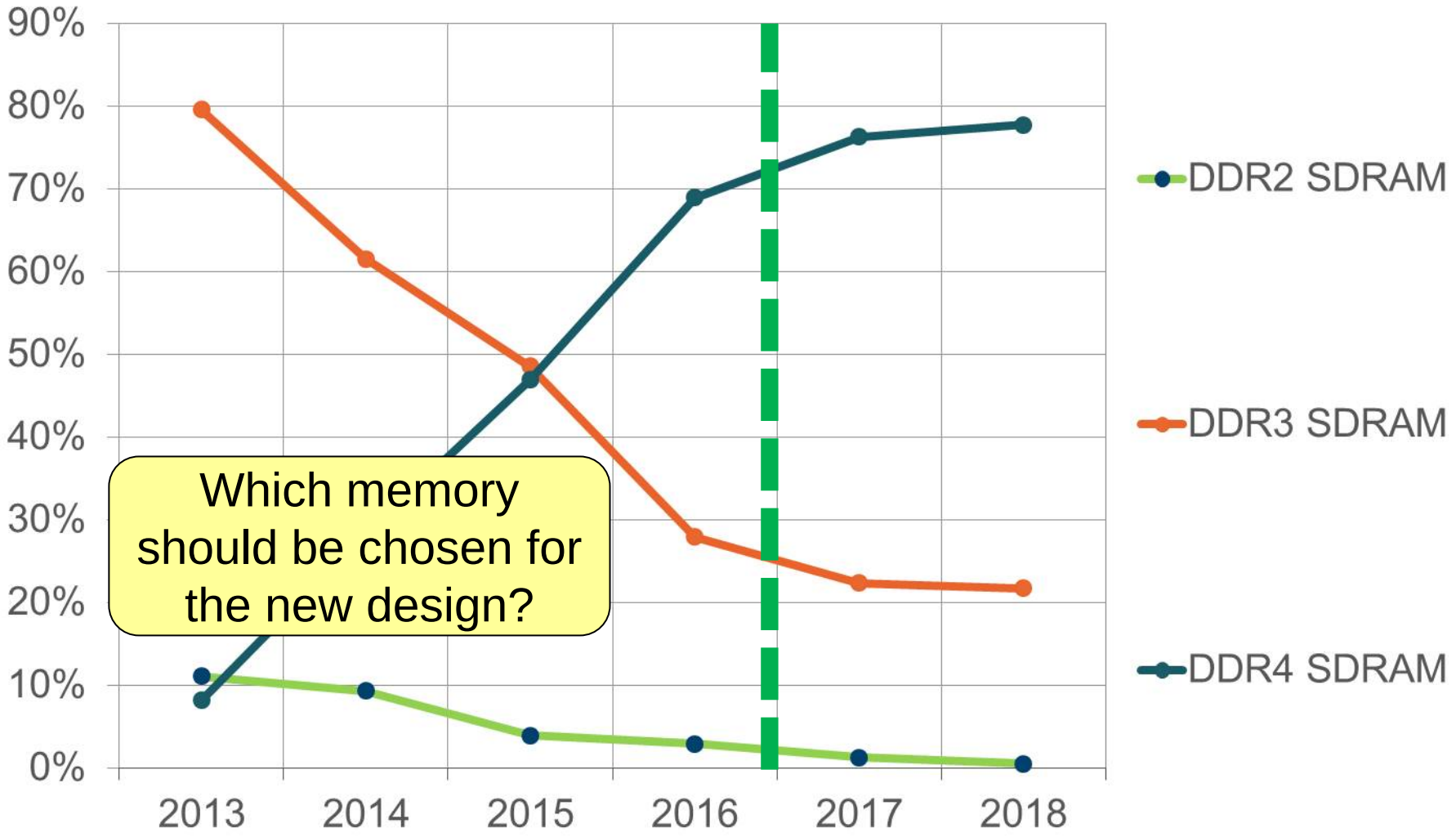

Source: Gartner (March 2014)

Objectives

- **Explore major differences between DDR4 and DDR3**
- **Know which memories are supported with UltraScale**
- **See how to start a DDR4 memory controller design in UltraScale using MIG**
- **Preview next generation memory interfaces**

Agenda

- **Technology differences: DDR4 vs. DDR3**
- **UltraScale memory interface features**
- **System design-in considerations for DDR4 with UltraScale**
- **Creating an UltraScale DDR4 memory controller**
- **Next generation memory**

Technology Differences: DDR4 vs. DDR3

Remember Slide 2?

DDR4 Advantages in

- **Power**
- **Performance**
- **Price**

Memory Interface Criteria

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- **DDR4 delivers in all three areas with UltraScale™ (compared to DDR3)**

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DDR3 vs. DDR4: Voltage and Power

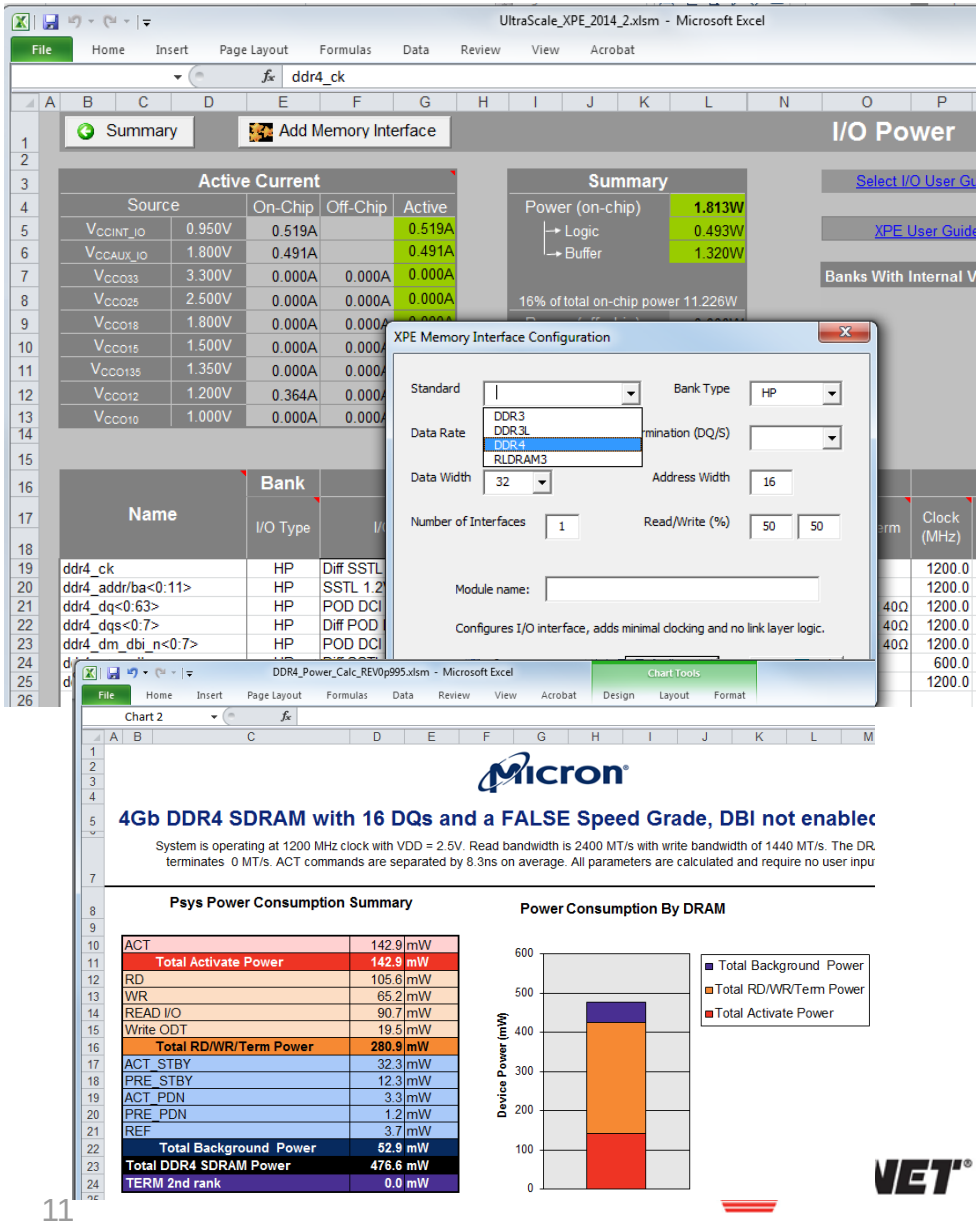
Features	DDR3/L	DDR4	DDR4 Improvements
V_{DD}/V_{DDQ}	1.5V/1.35V	1.2V	25% reduction to DDR3
V_{PP}	internal word-line charge pumps	2.5V	More cost-effective and allows lower $V_{DD/Q}$
V_{TT}	½ V_{DD}/V_{DDQ} sink/source	½ V_{DD}/V_{DDQ} sink/source	25% reduction to DDR3
V_{REF} Inputs	½ V_{DD}/V_{DDQ} DQ and CA	½ V_{DD}/V_{DDQ} CA only	V_{REFDQ} is internal
DQ Termination	SSTL	Pseudo-Open Drain (POD)	Reduces termination current
Example: Power (IDD7)	339mW (DDR3L, 30nm, 4Gb, 1866MT/s)	247mW (DDR4, 30nm, 4Gb, 1866MT/s)	27% less power

FPGA Power Savings

Interface	Rate/Width	IO/PHY Power	% Savings
DDR3, 7-Series	1866 Mb/s, 32-bit	1.41 W	-
DDR4, UltraScale	1866 Mb/s, 32-bit	0.94 W	33%
DDR4, UltraScale	2400 Mb/s, 32-bit	1.10 W	22%

DDR4 Power Circuit Design – $V_{DD/Q}$ and V_{PP}

- **V_{DD} and V_{DDQ} = 1.2 V**
  - +/- 5% tolerance
  - May share a single supply
  - Also may share supply with FPGA V_{CCO}
  - Switching regulators are a good choice
  - Single shared supply may require multiple amps
  - Use Power Calculators to estimate
- **V_{PP} = 2.5 V**
  - +/-10% tolerance
  - Check DDR4 datasheet for current requirements
  - ~30 mA for one 4Gb device



DDR4 Power Circuit Design – V_{TT} and V_{REF}

- **V_{TT} and V_{REF} value are dictated by $V_{DD/Q}$**
  - Must be 50% of your $V_{DD/Q}$ voltage
  - V_{TT} must be sink/source

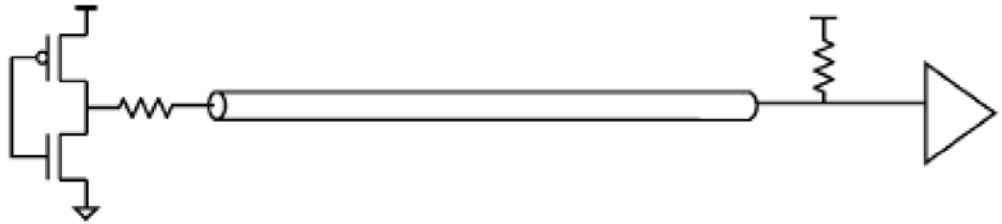
- **V_{TT} / V_{REF} dedicated termination regulators**
  - TPS5120x family from Texas Instruments
  - NCP51199 from OnSemi
  - MAX1510 from Maxim Integrated

- **V_{REF} alternatives**
  - Low noise linear regulators
  - Resistor divider as seen on Xilinx KCU105
  - Internal V_{REF} required for UltraScale

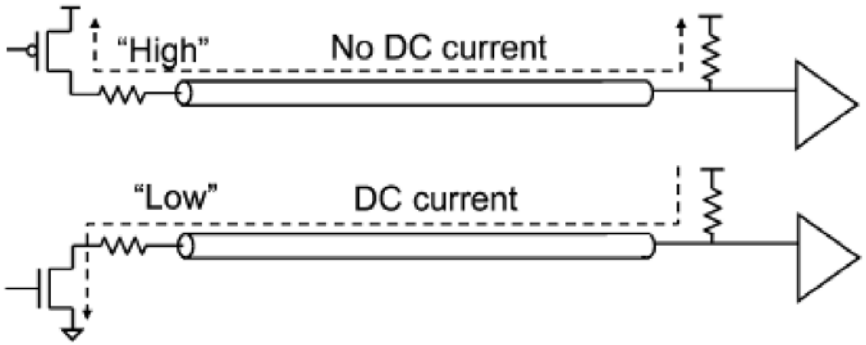
- **V_{TT} alternative**
  - Synchronous switching regulators able to sink current
  - Needs to accurately regulate to 50% of your $V_{DD/Q}$

DDR4 Termination

- **Command/Address uses SSTL (same as DDR3)**
- **Data uses Pseudo Open Drain (POD) 1.2V**



- **POD driver has**
  - strong pull-down strength
  - weak pull-up strength
    - True open-drain has no pull-up strength
- **Requires external pull-up resistor to HIGH voltage**
  - In practice, this is accomplished internally
    - DCI in FPGA
    - ODT in DDR4 device
- **Advantage: no DC current during high drive**



DDR3 vs. DDR4: Performance in UltraScale

Features	DDR3/L	DDR4	DDR4 Improvements
Data rate (Mb/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, 2667, 3200	50% faster

DDR3 vs. DDR4: Performance in UltraScale

Features	DDR3/L	DDR4	DDR4 Improvements
Data rate (Mb/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, ~~2667, 3200~~	13% ~~50%~~ faster

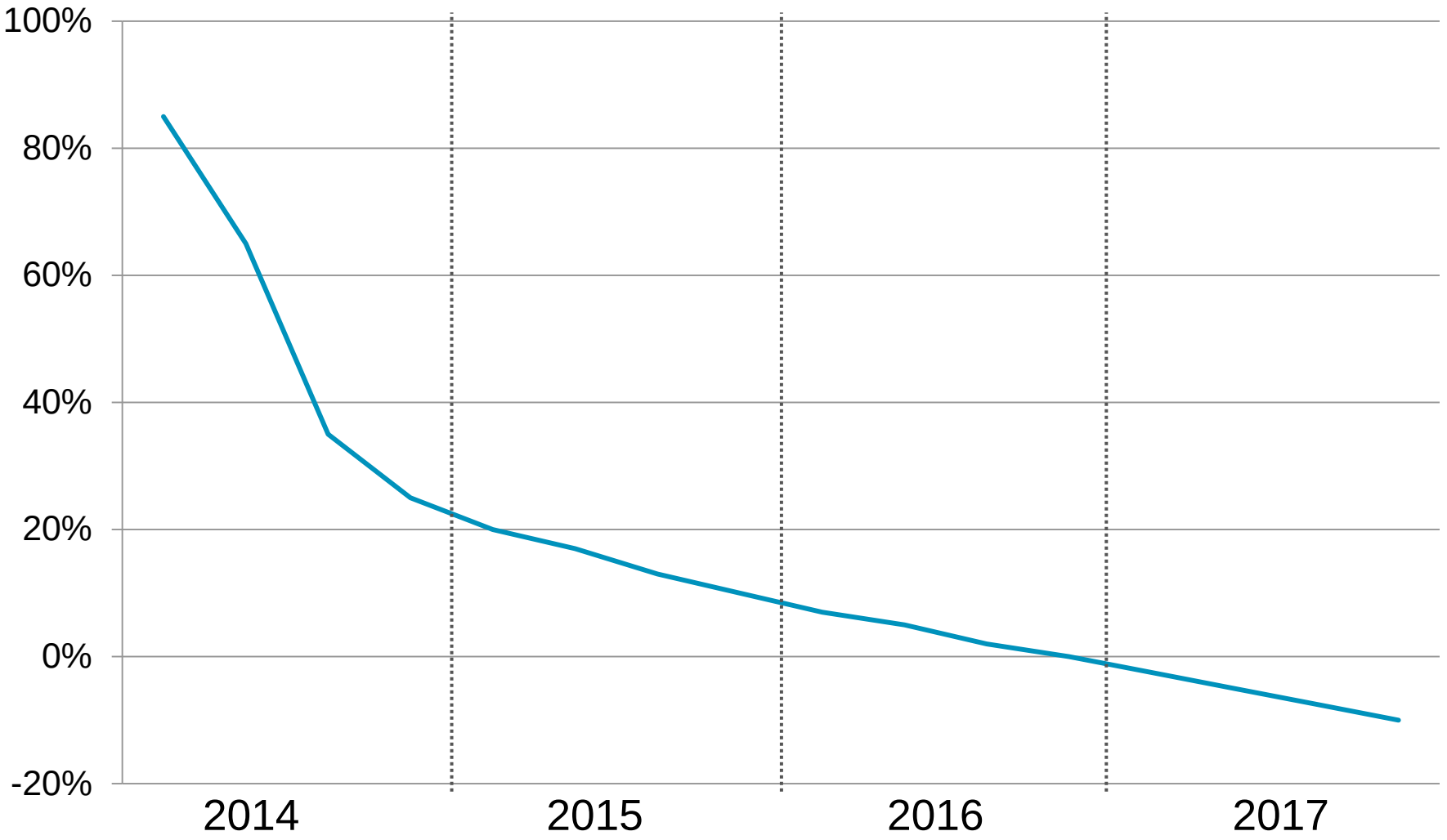
* Not supported in UltraScale

DDR3 vs. DDR4: Performance in UltraScale

Features	DDR3/L	DDR4	DDR4 Improvements
Data rate (Mb/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, ~~2667, 3200~~	13% ~~50%~~ faster
Densities	512Mb to 8Gb	2Gb to 16Gb	2x density in a single chip
Internal Banks	8	16 (x4,x8) 8 (x16)	More banks (x4, x8)
Bank groups	0	4 (x4, x8) 2 (x16)	Faster burst accesses

* Not supported in UltraScale

DDR4 vs. DDR3: Price Premium



* Estimate courtesy Micron

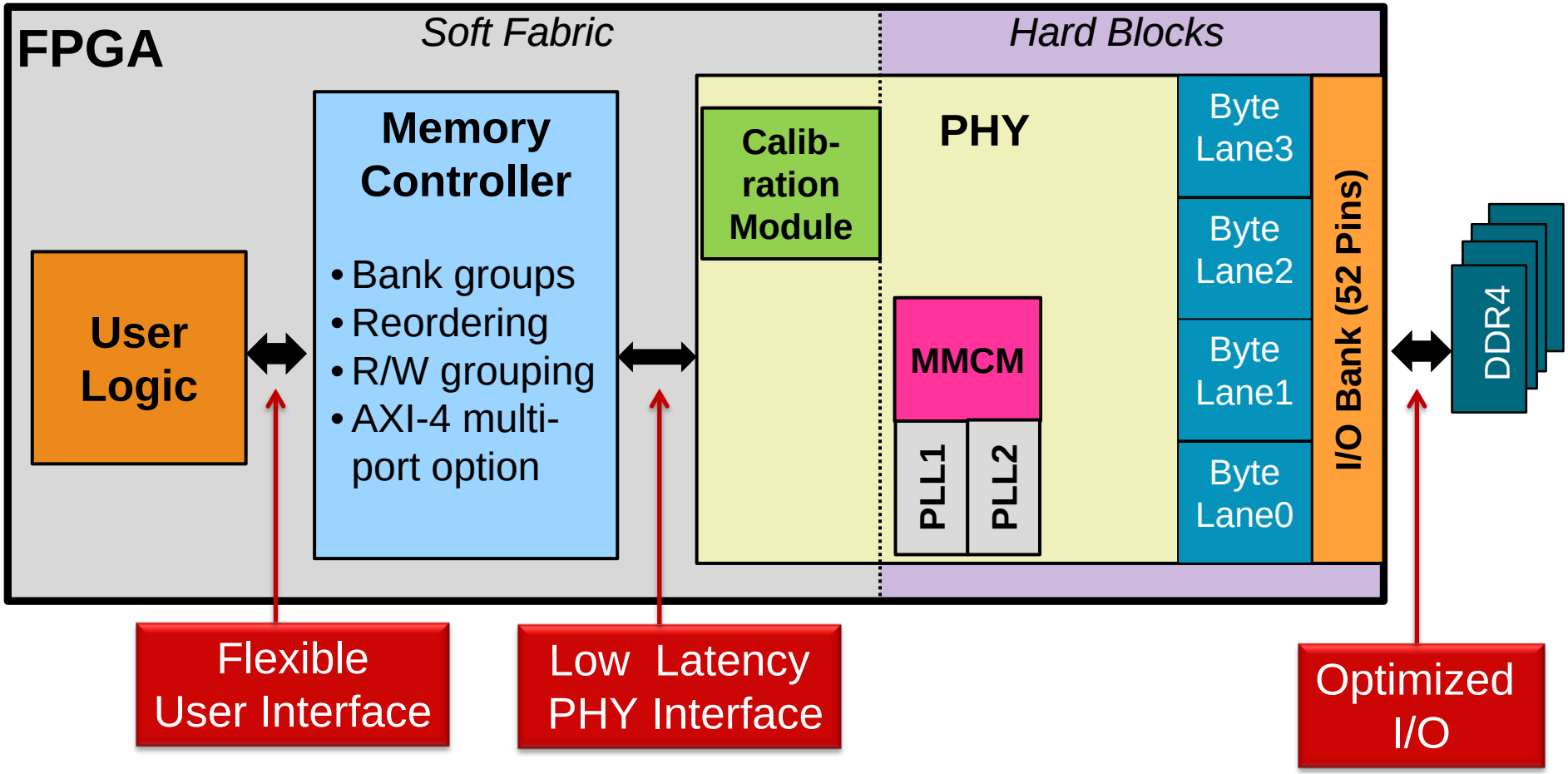
UltraScale Memory Interface Features

UltraScale Memory Interface Support

Memory	UltraScale Support
DDR4	1200 MHz
DDR3	1067 MHz
DDR3L	933 MHz
LPDDR3	TBD
QDR II+ (Xtreme)	633 MHz
QDR IV	TBD
RLDRAM 3	1066 MHz

Speed grade and package dependent

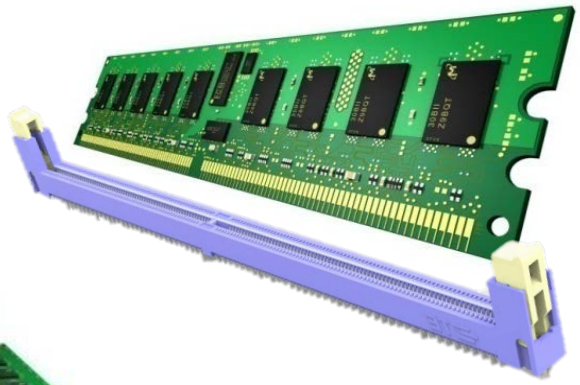
UltraScale Memory Interface Architecture



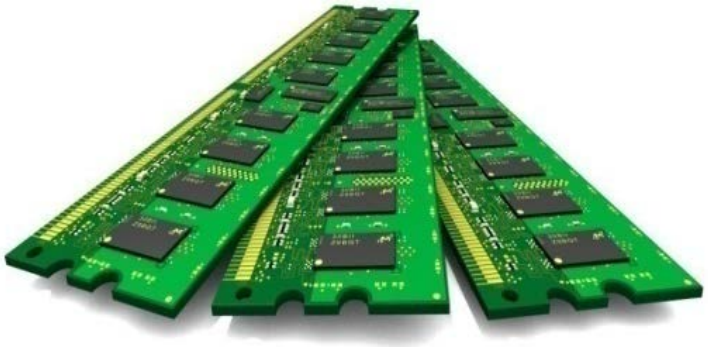
UltraScale DDR4 DIMM Support

- **x16, x8, and x4-based DIMMs**

- **Single, dual, and quad rank DIMMs**



- **DIMM types supported**
  - SODIMM
  - UDIMM
  - RDIMM



Micron®

TE connectivity

Xfest

AVNET®

Vivado® DDR4 DIMM Support

DDR4 DIMM Type	Vivado Support Schedule*
SODIMM (1R, 2R)	2014.3
UDIMM (1R, 2R)	2014.3
RDIMM (1R, 2R)	2015.1
RDIMM (4R)	2015.2

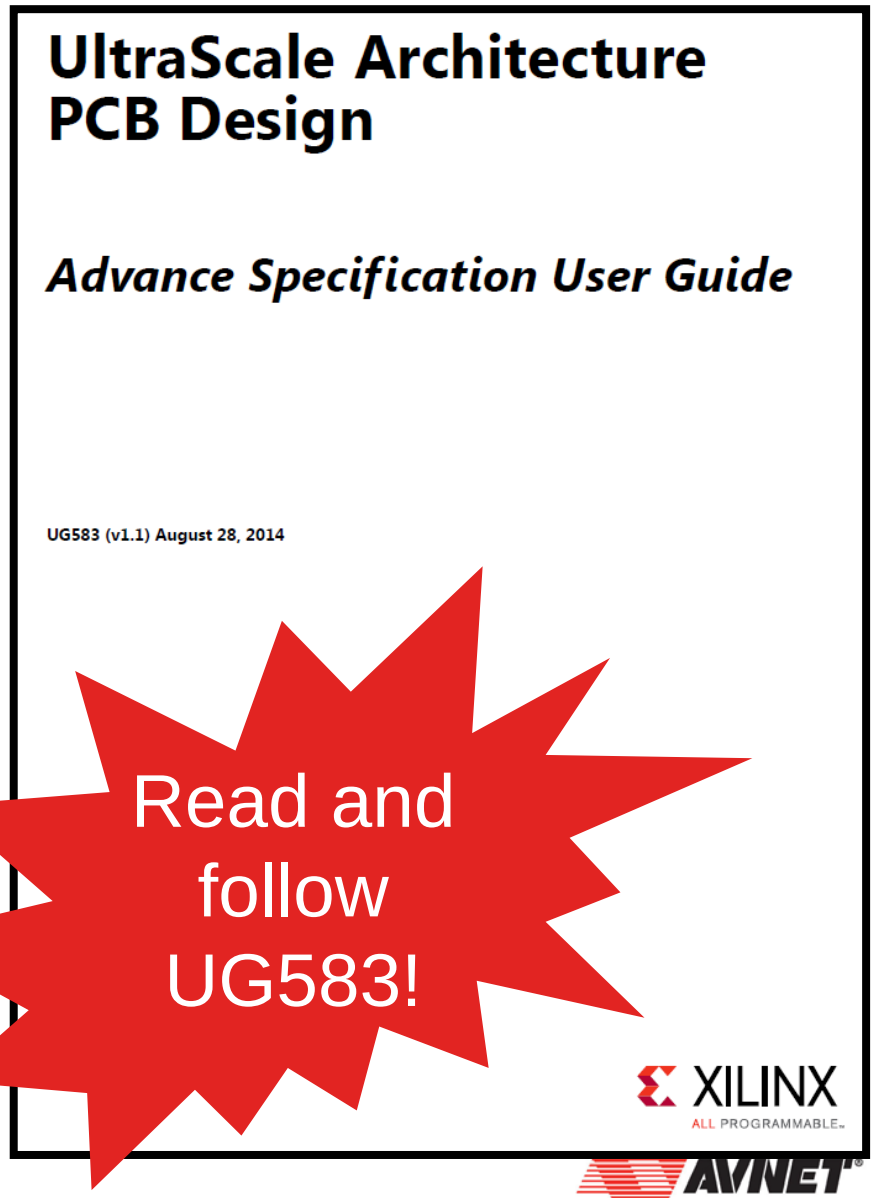
Notes:

- Release version for support is subject to change
- No current plans for an UltraScale development board with DDR4 DIMM

System Design-in Considerations for DDR4 with UltraScale

High-Speed PCB Design

- **Understand transmission line theory**
- **Match trace lengths**
- **Control impedances**
- **Use proper termination**
- **Utilize best practice power supply design**
  - Bypass properly
  - Avoid crossing splits in the power plane
- **Reduce noise on V_{REF}**
- **Engineer the layout to minimize crosstalk**



High-Speed PCB Design

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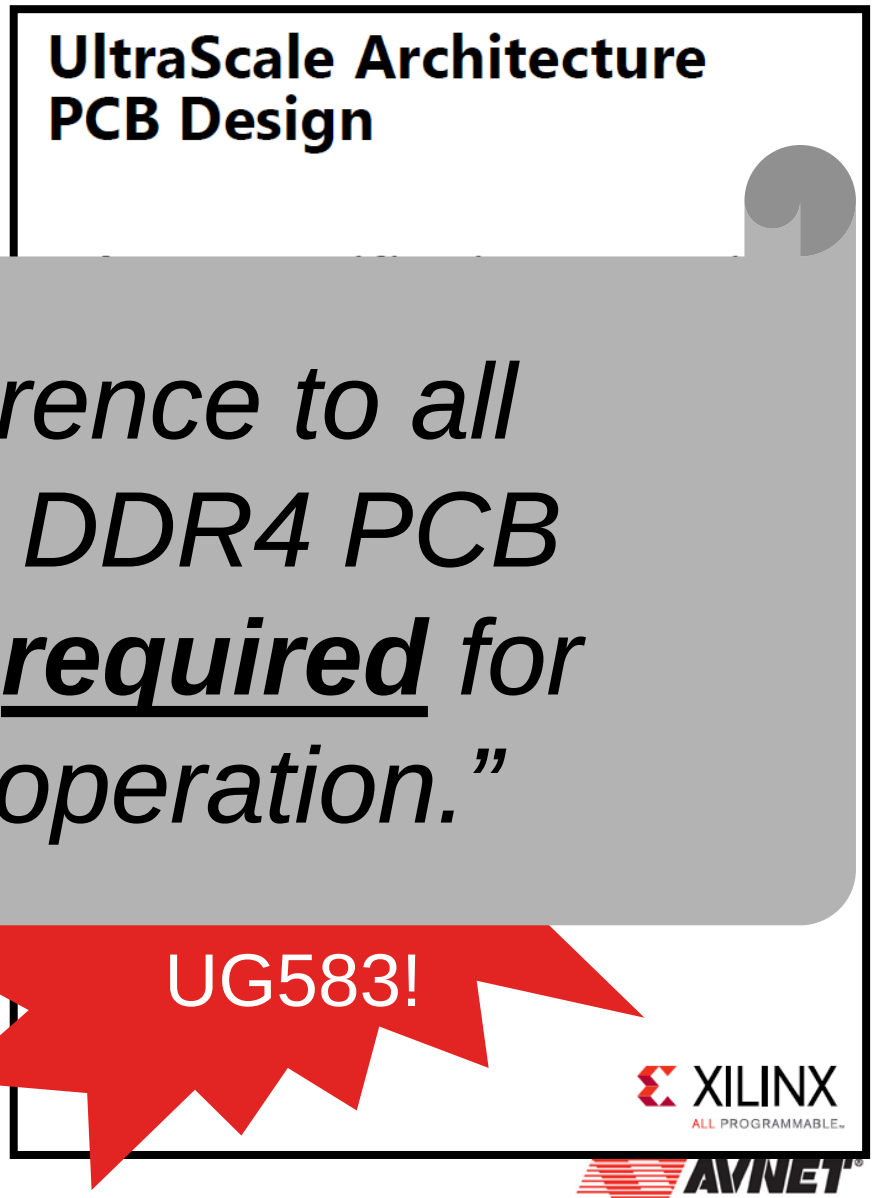
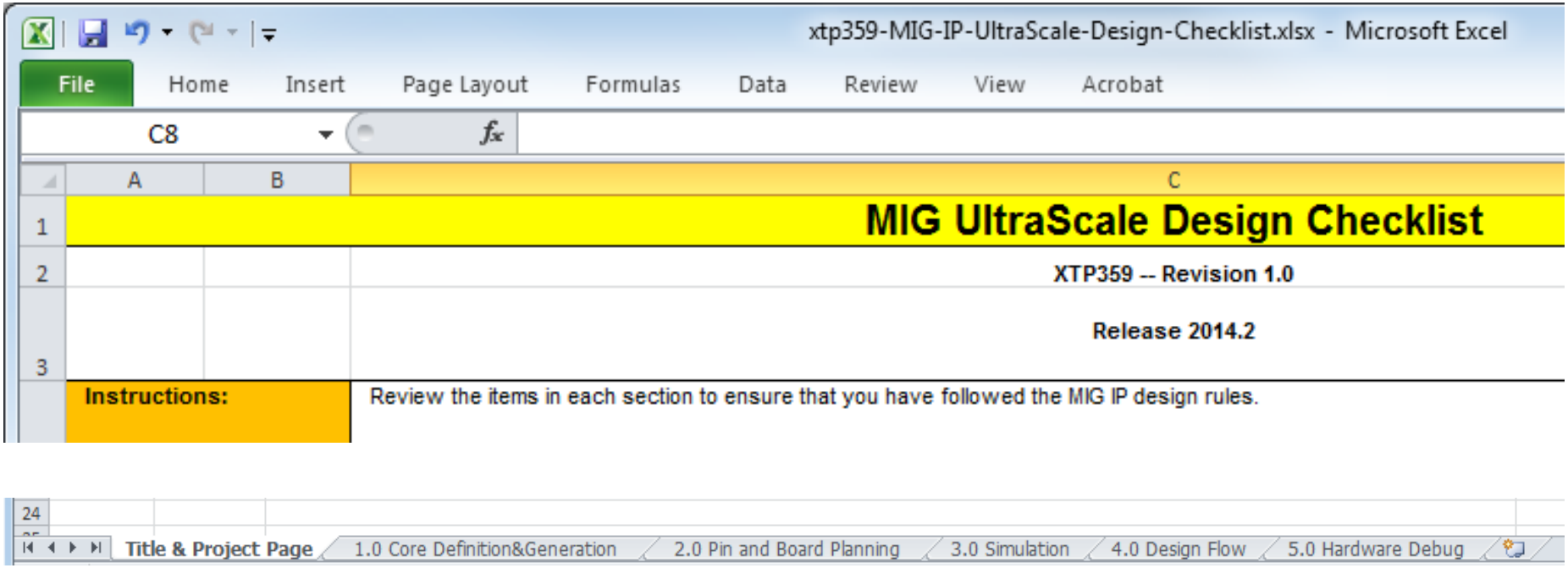


*"Strict adherence to all documented DDR4 PCB guidelines is **required** for successful operation."*

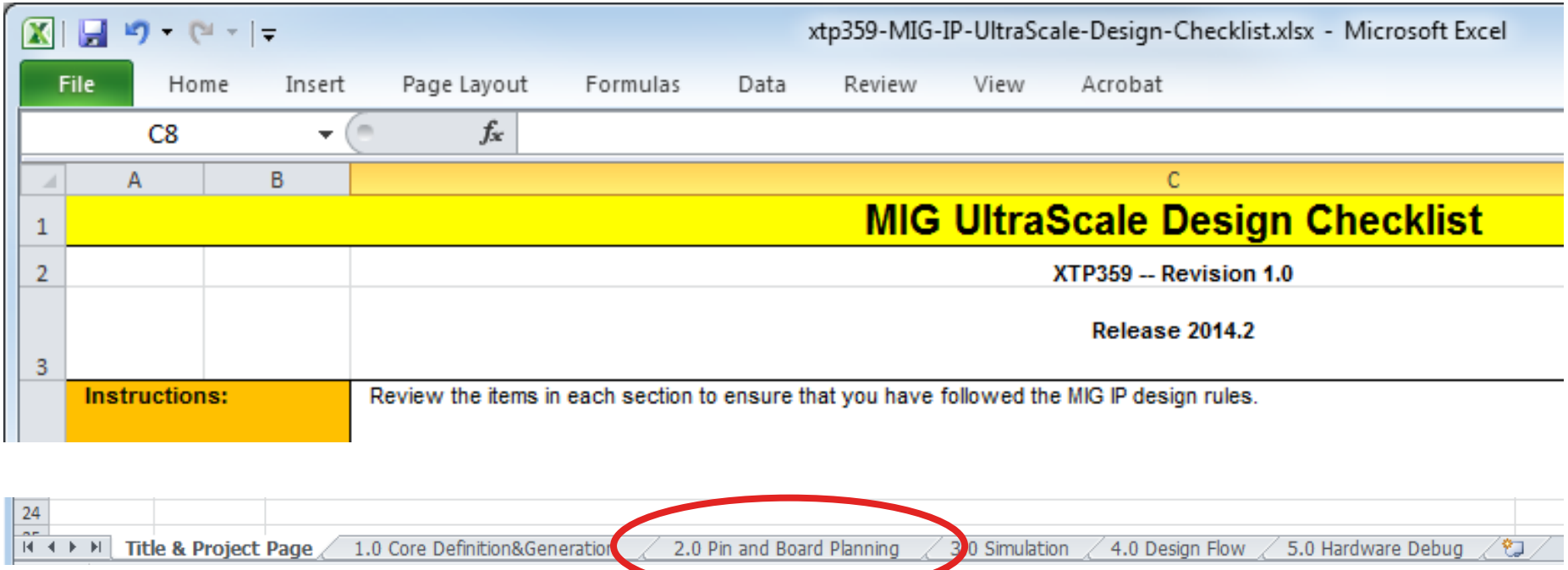
- **Engineer the layout to minimize crosstalk**

UG583!

DDR4 Design Checklist – XTP359



DDR4 Design Checklist – XTP359



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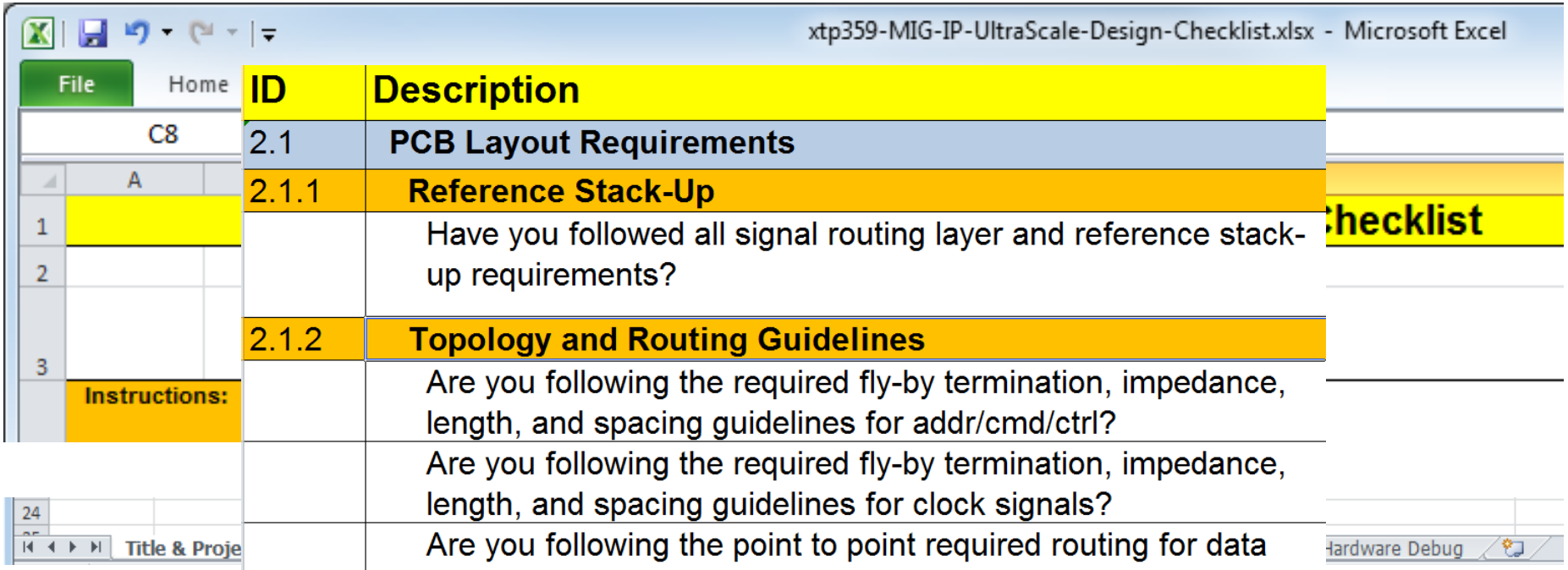
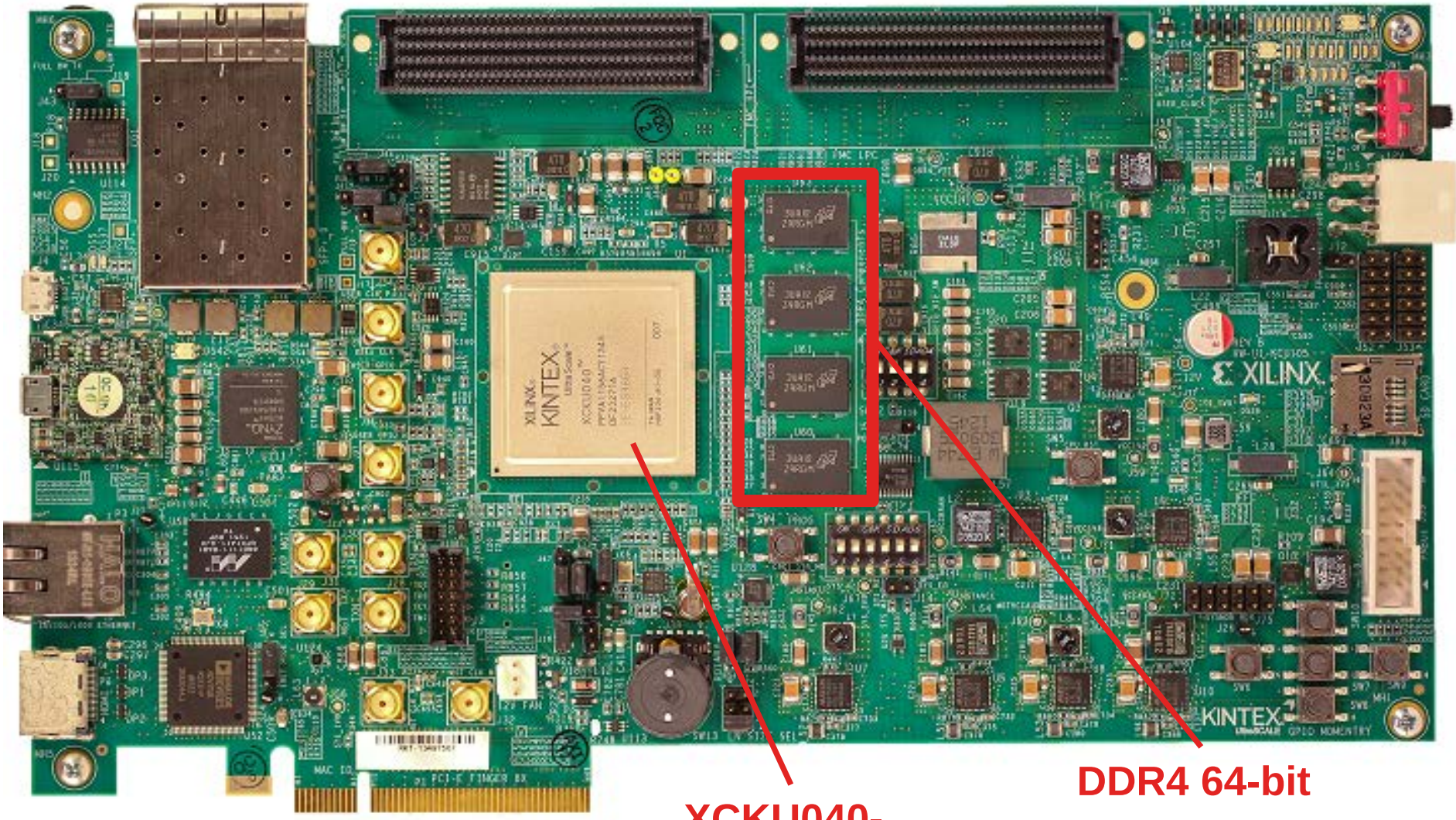


ID	Description
2.1	**PCB Layout Requirements**
2.1.1	**Reference Stack-Up**
	Have you followed all signal routing layer and reference stack-up requirements?
2.1.2	**Topology and Routing Guidelines**
	Are you following the required fly-by termination, impedance, length, and spacing guidelines for addr/cmd/ctrl?
	Are you following the required fly-by termination, impedance, length, and spacing guidelines for clock signals?
	Are you following the point to point required routing for data signals?
	Are you following the required length routing constraints?
	Are you following the required length matching routing constraints?
	Package Delays must be included in length matching. Package delays can be found within the Vivado Pinout Table.
	Are you following MIG routing guidelines?

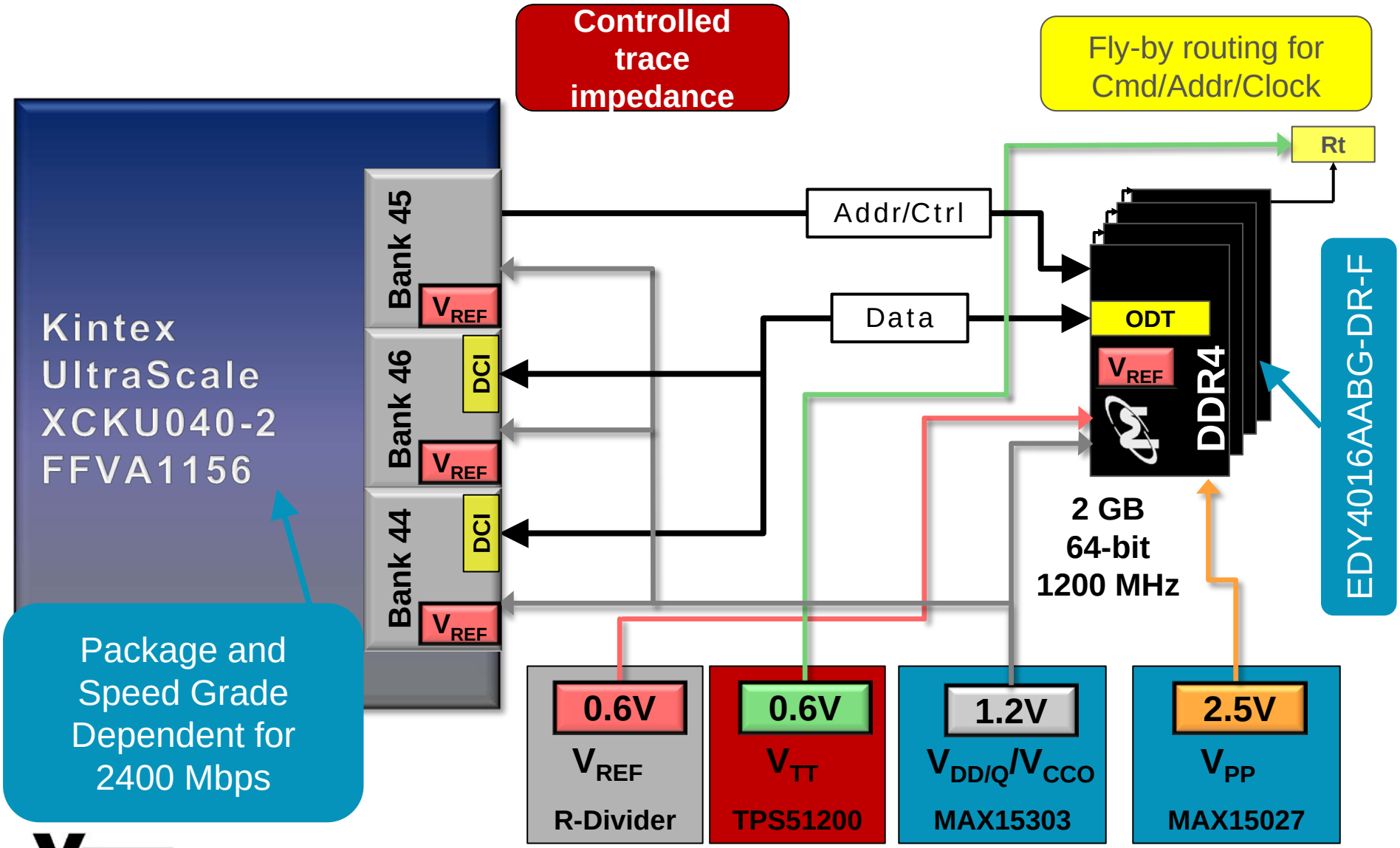
Design Example: KCU105 Board



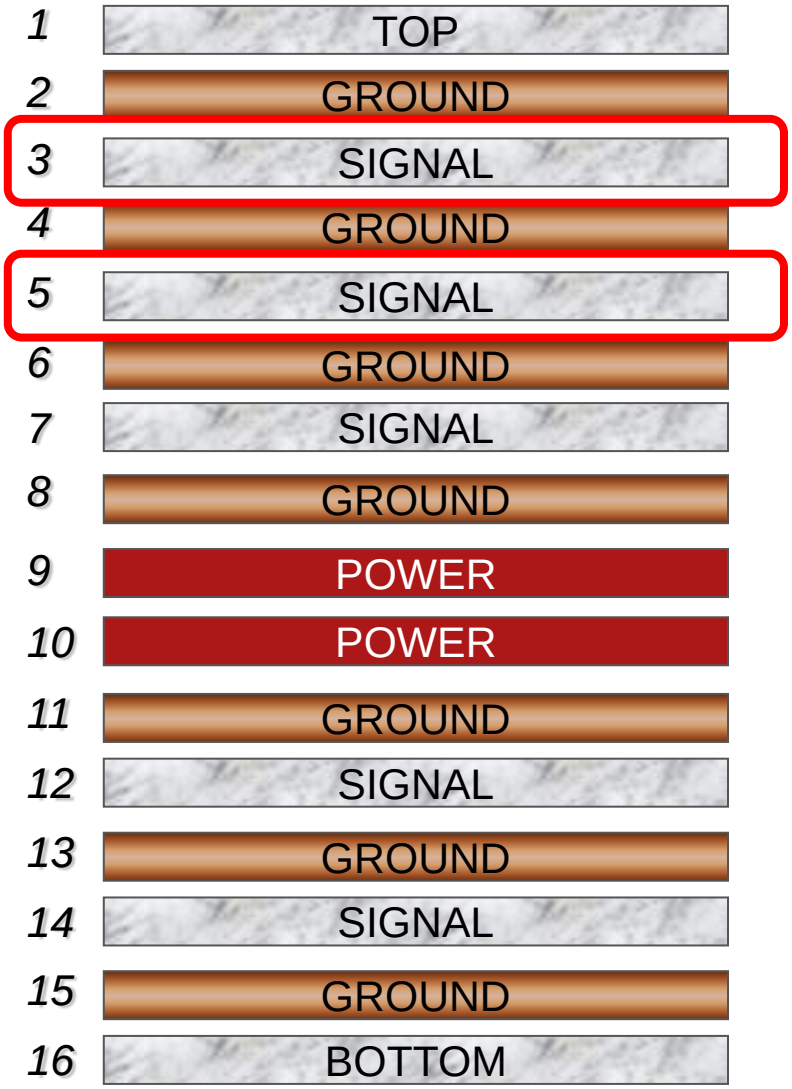
XCKU040-
2FFVA1156

DDR4 64-bit
EDY4016AABG-DR-F

KCU105 Memory Interface PCB Design



Stack-up Recommendation (KCU105)



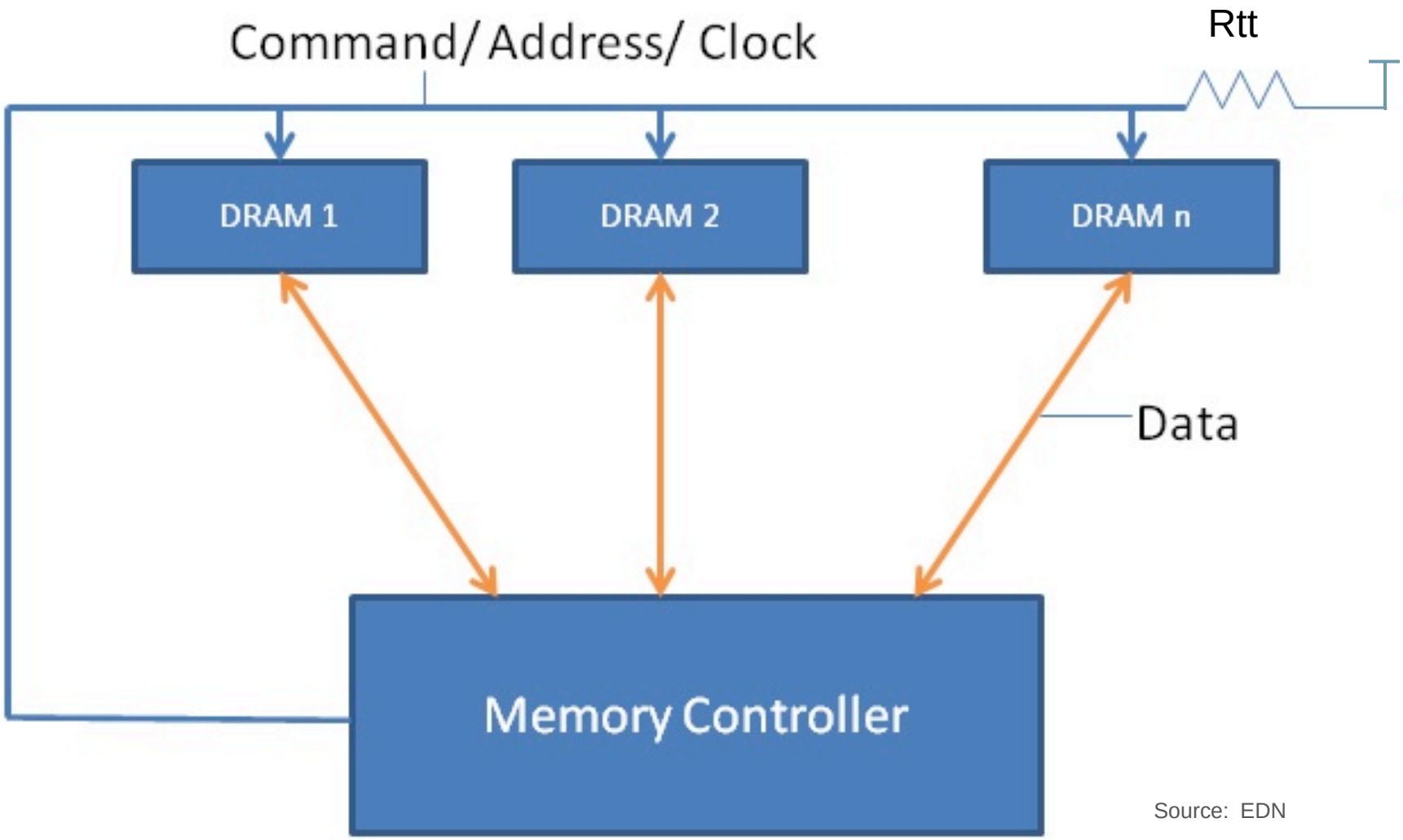
To achieve highest memory interface performance

- DDR4 signals must be routed on the top signal layers, that is, L3/L5

Notice

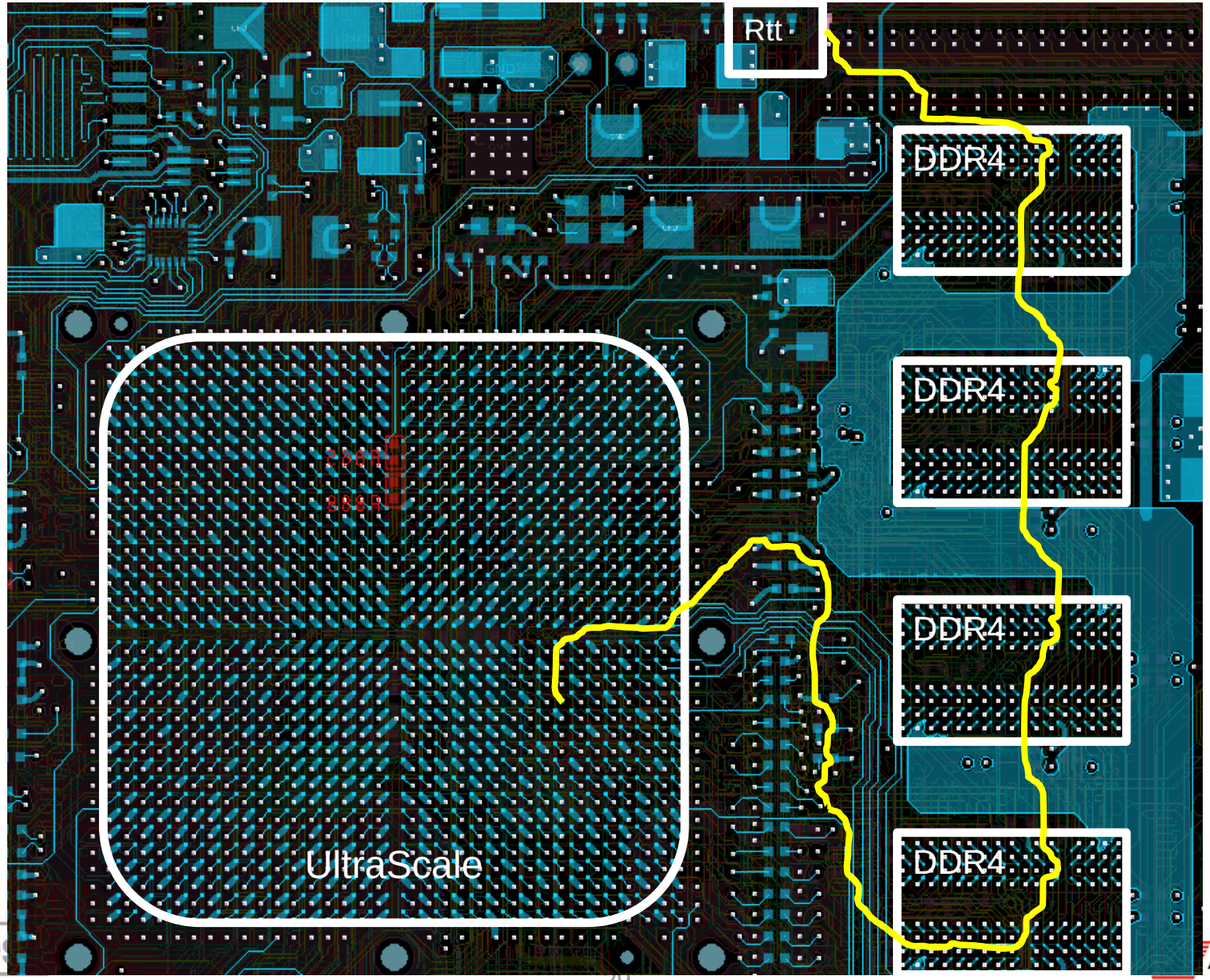
- All DDR4 components and UltraScale should be on the top side
- No adjacent signal layers
- All reference planes are GROUND

Fly-By Routing



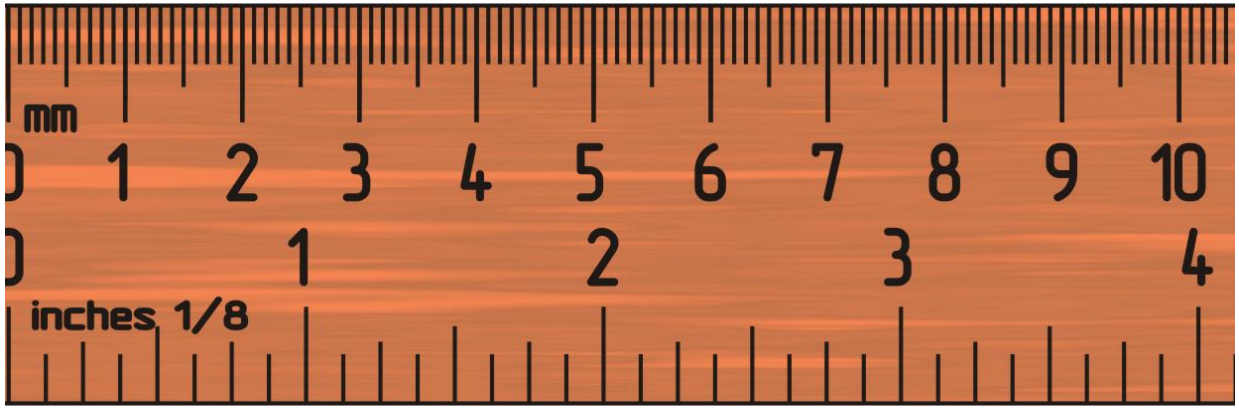
Source: EDN

KCU105 Fly-by

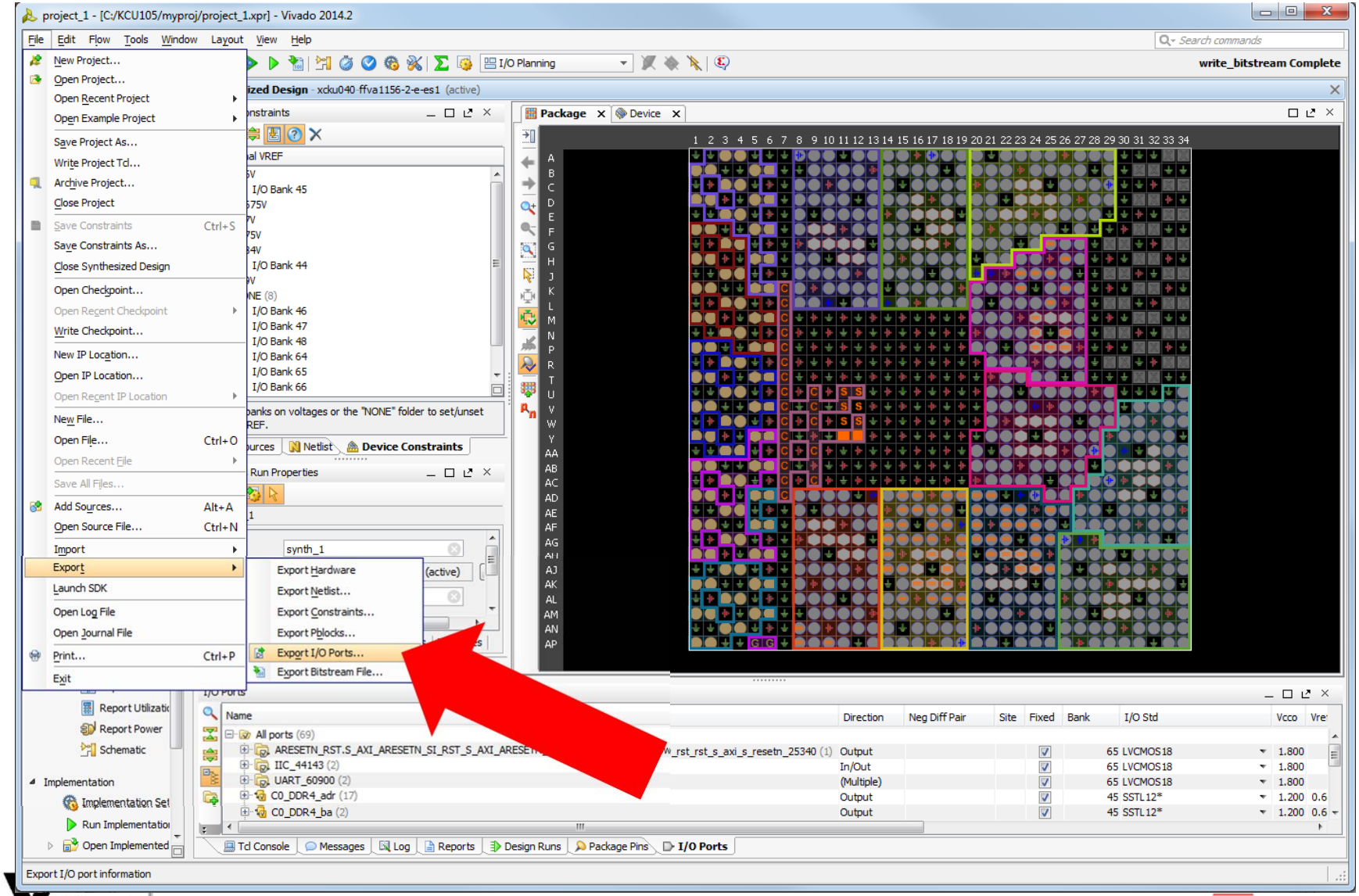


Trace Length Matching

- **All DDR4 signals have min/max length requirements**
- **All DDR4 signals must be matched within groups**
- **Example: DQs within a data group**
  - Match within +/- 15 mil
  - MUST include internal package delays
    - In Vivado, open synthesized design, then…



File → Export → Export I/O Ports



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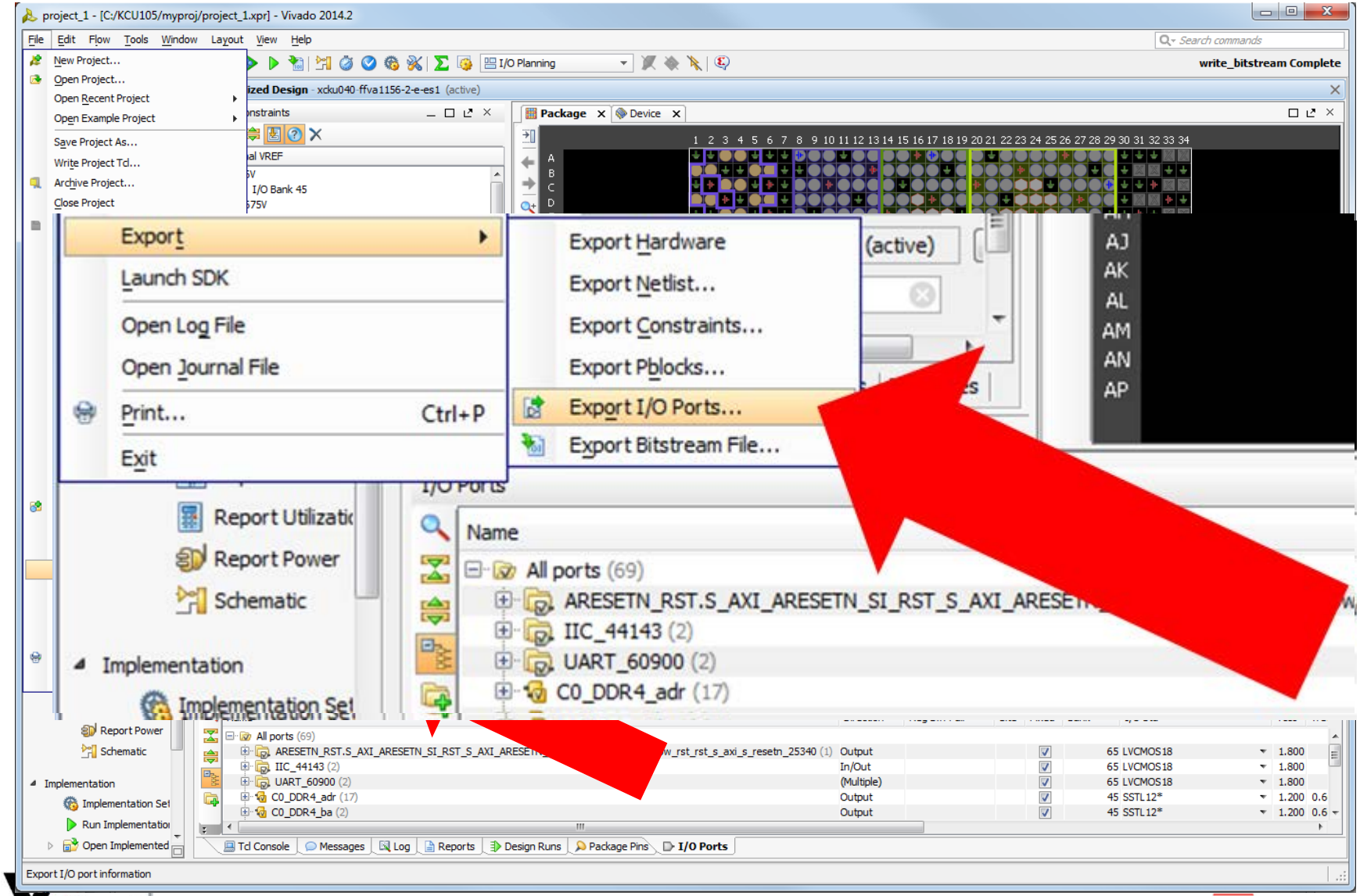
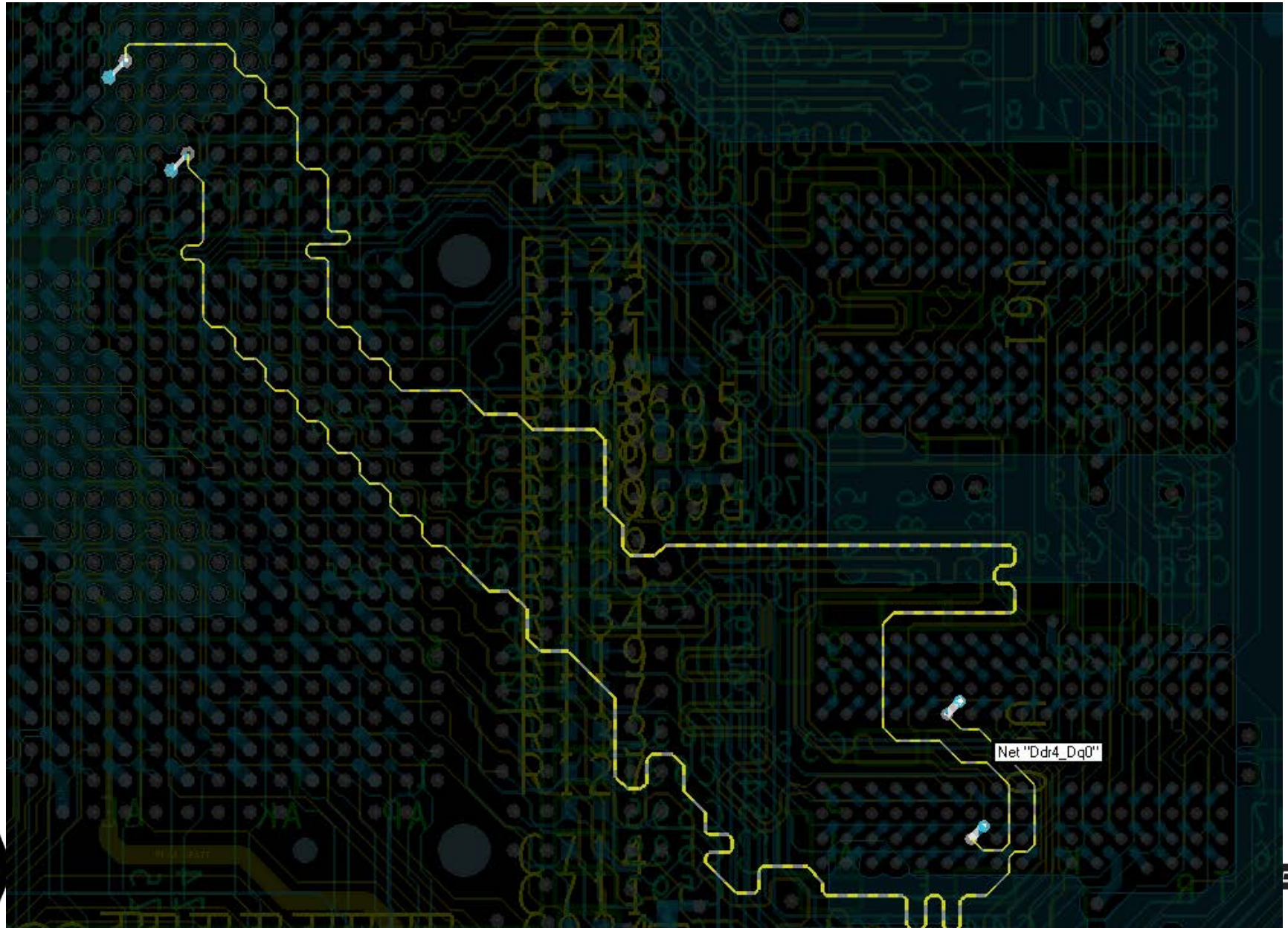


KCU105 Trace Length Matching Example

- **PCB flight time**
  - Microstrip → 136 ps/in = 0.136 ps/mil
  - Stripline → 170 ps/in = 0.17 ps/mil
- **Specification: +/-15 mil = +/- 2.55 ps**

Signal	UltraScale Pin	Package Flight Time (ps)	KCU105 Flight Time (ps)			Total (ps)	Diff-erence
			Top	L5	Top		
DQ0	AE23	70.274	3.944	422.957	3.029	500.20	1.79 ps
DQ1	AG20	87.335	3.944	404.102	3.029	498.41	

KCU105 Routing DQ0 and DQ1



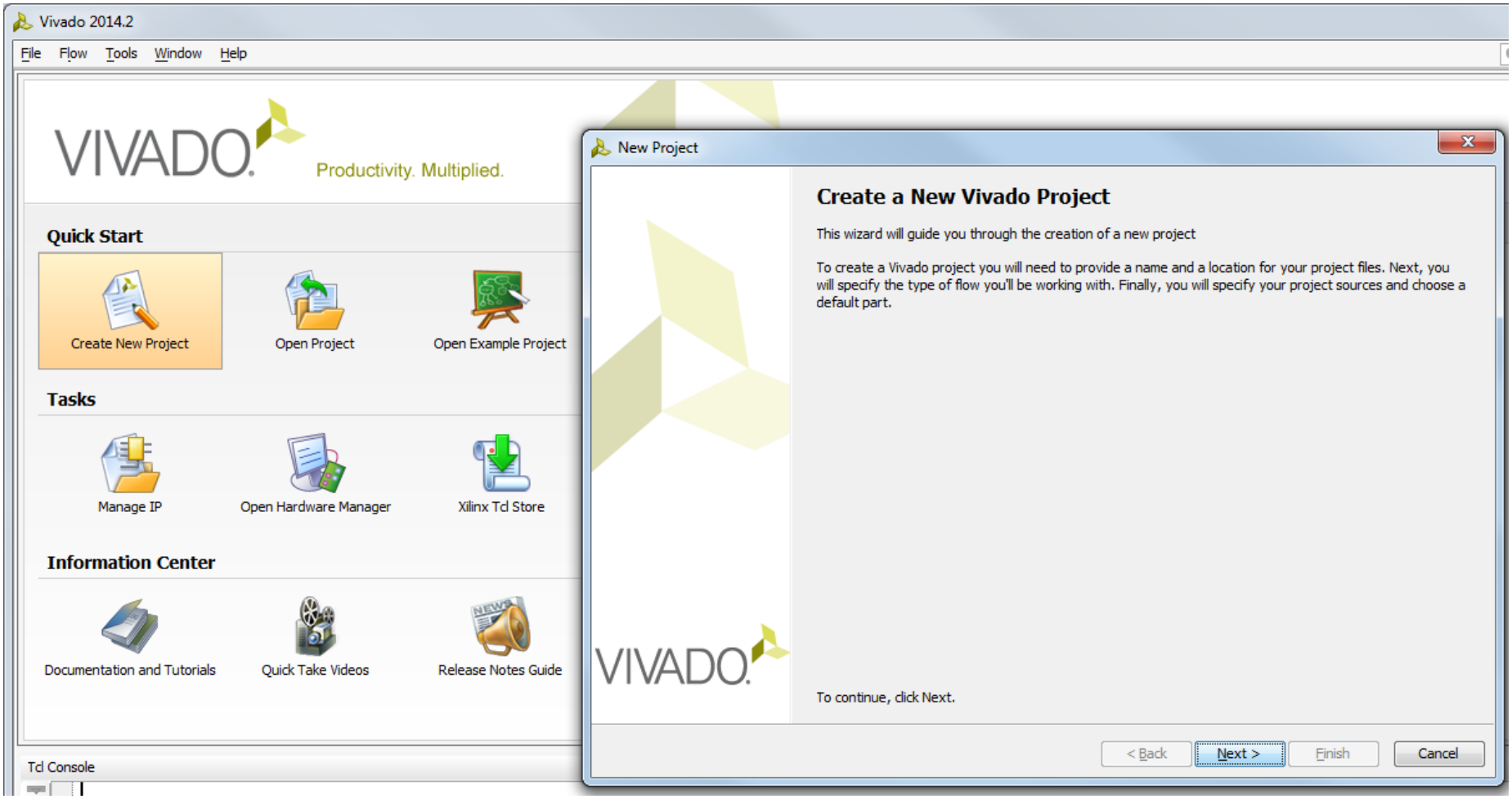
Creating an UltraScale DDR4 Memory Controller

Generating the Xilinx MIG DDR4 Controller

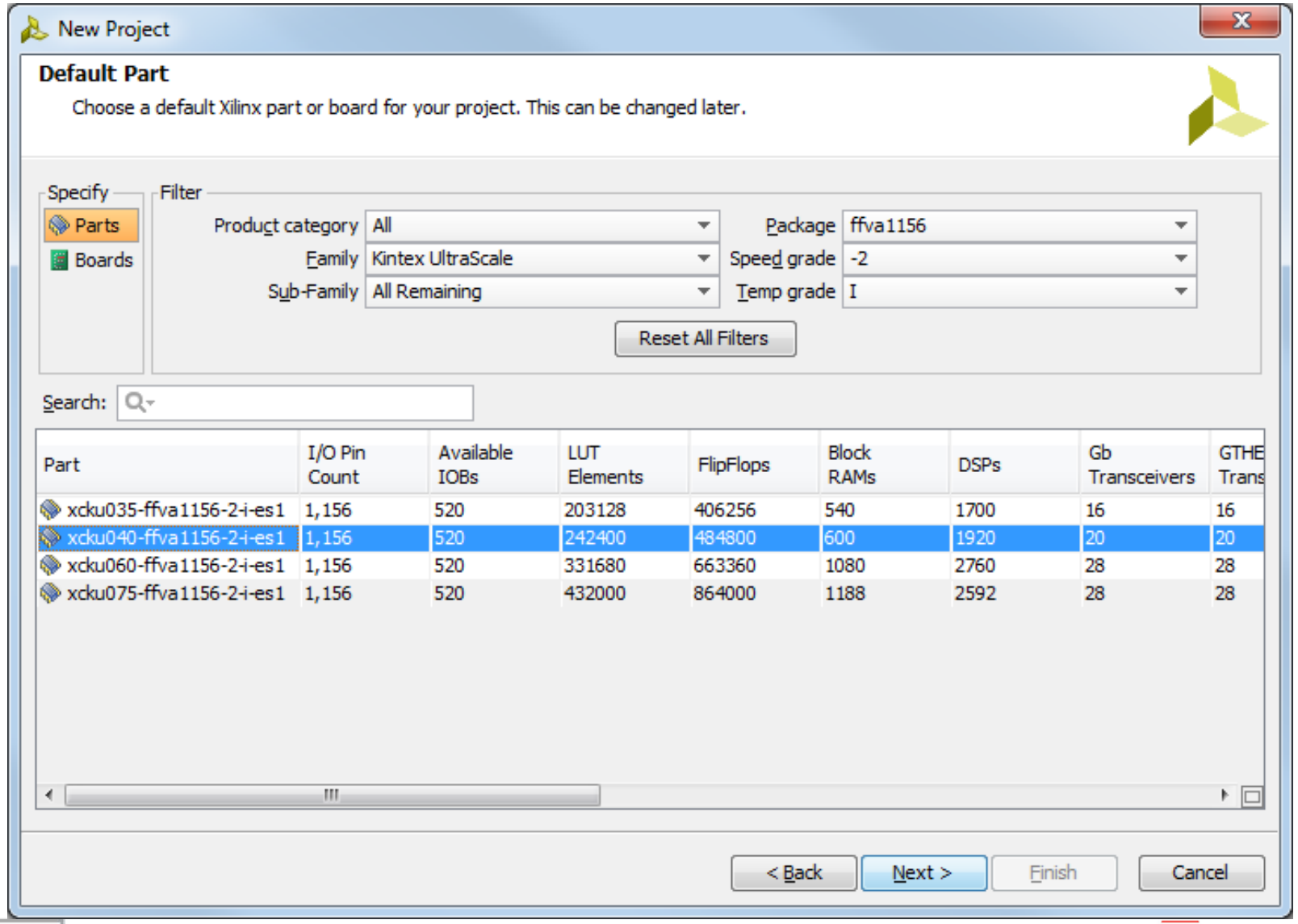
- **Memory Interface Generator (MIG)**
  - Launched from Vivado IP Catalog
  - Interface parameter selection
    - Device, burst length, data interleaving, re-ordering

- **Generated outputs**
  - HDL Code: Verilog (no VHDL)
    - User interface: AXI or User
  - Simulation support
  - Build parameters
  - Example design
    - Simulate or synthesize

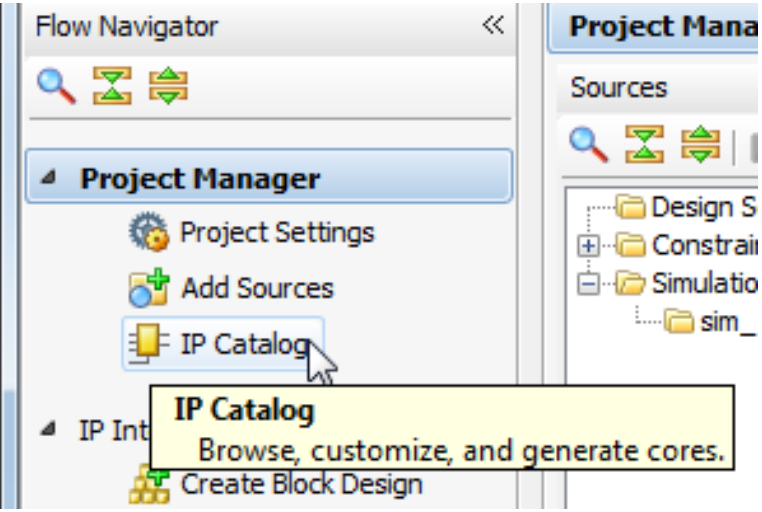
MIG Demo – Create New Project



MIG Demo – Select Kintex UltraScale Device



MIG Demo – Launch IP Catalog, Select MIG



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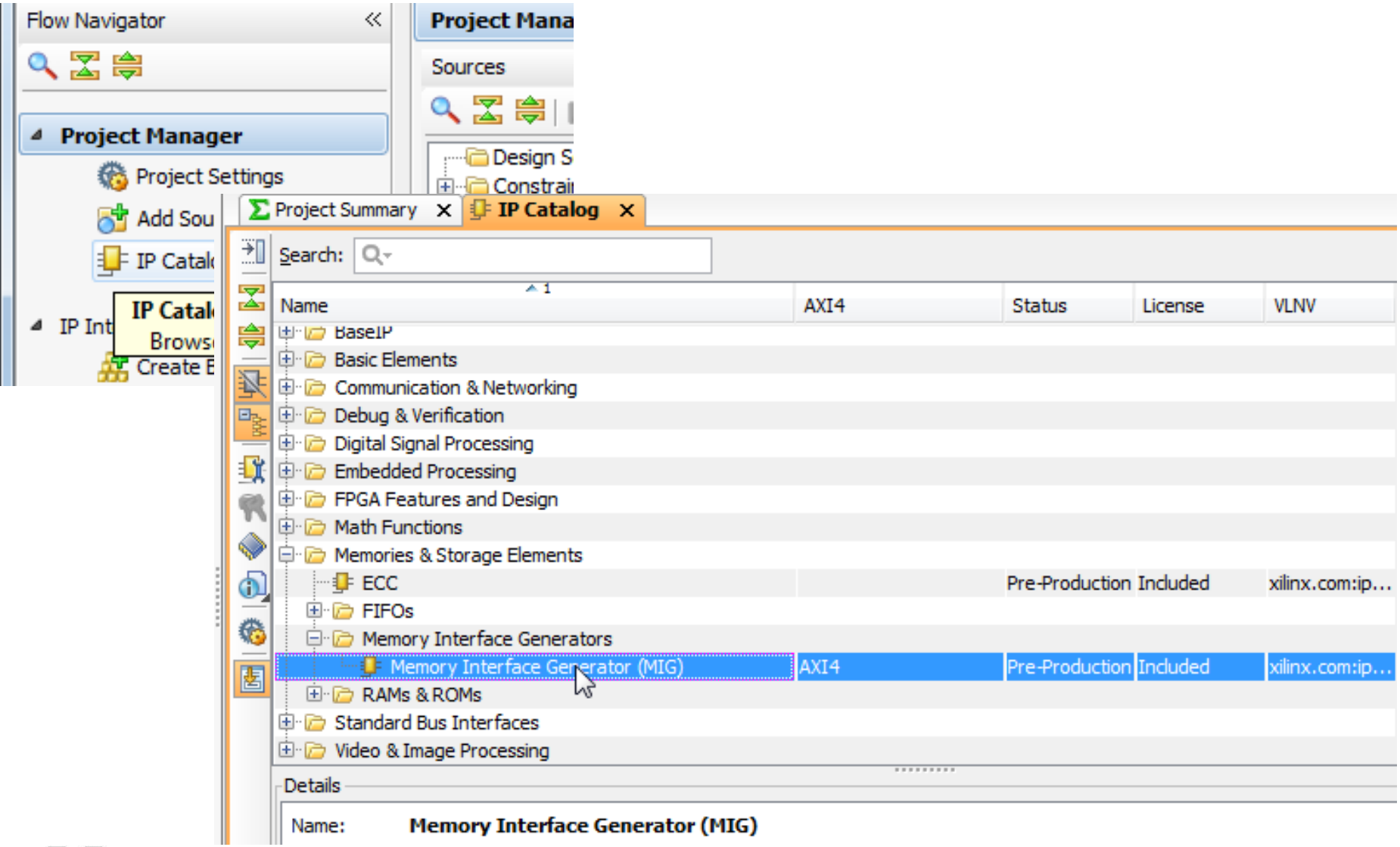
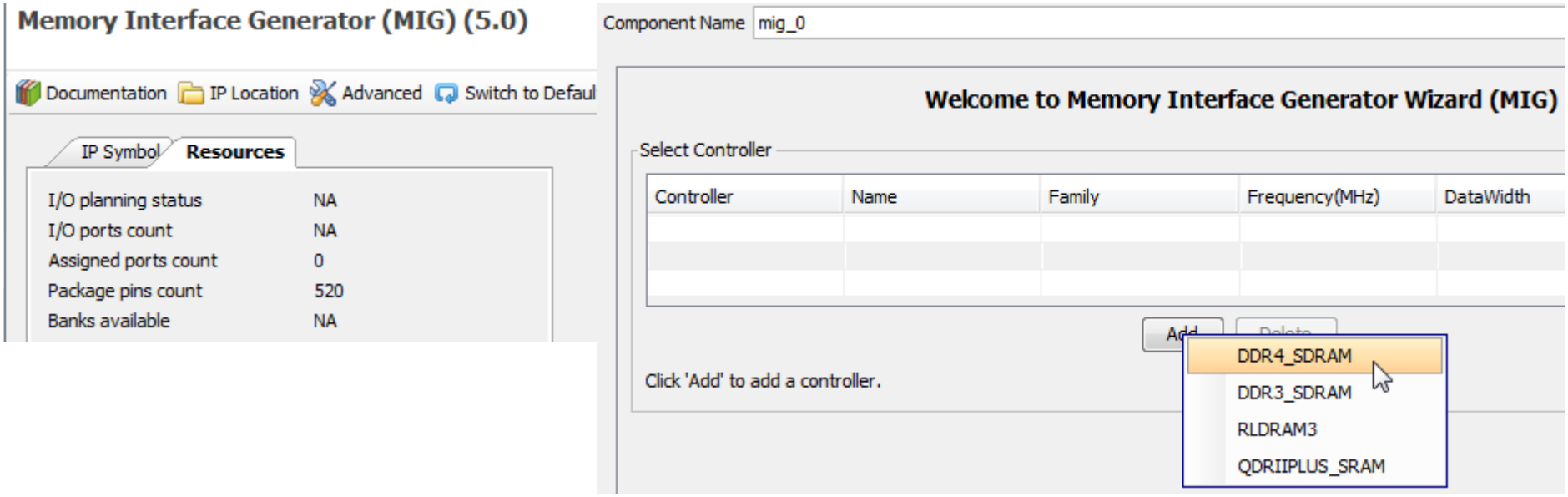


MIG Demo – Add DDR4 SDRAM Interface



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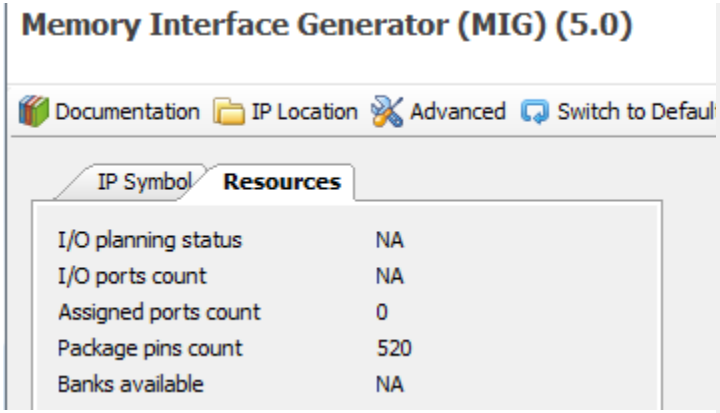
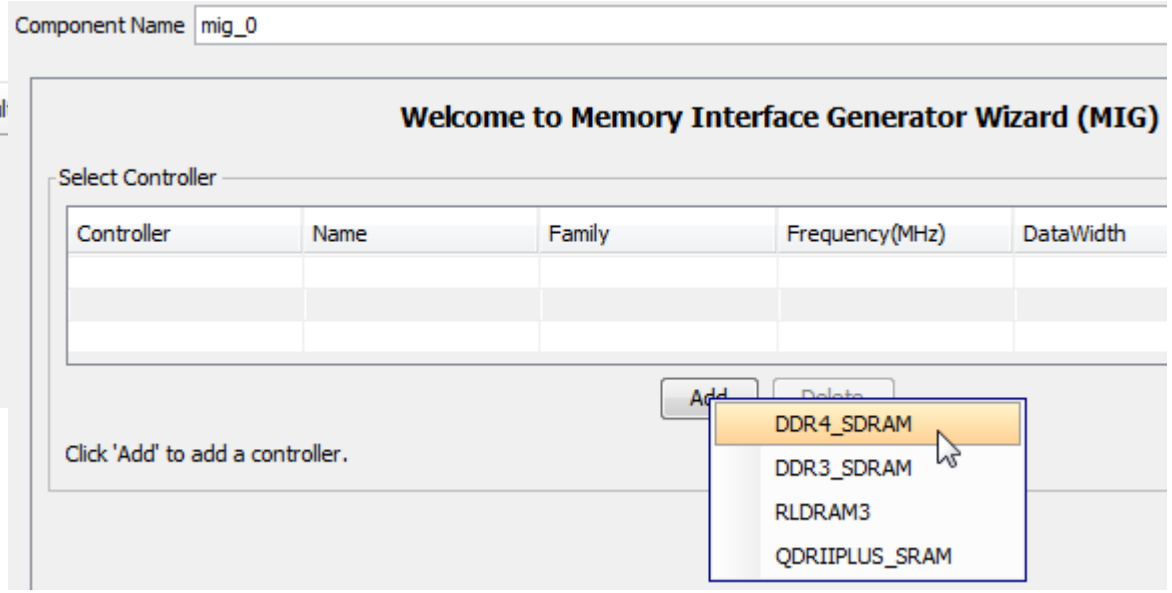
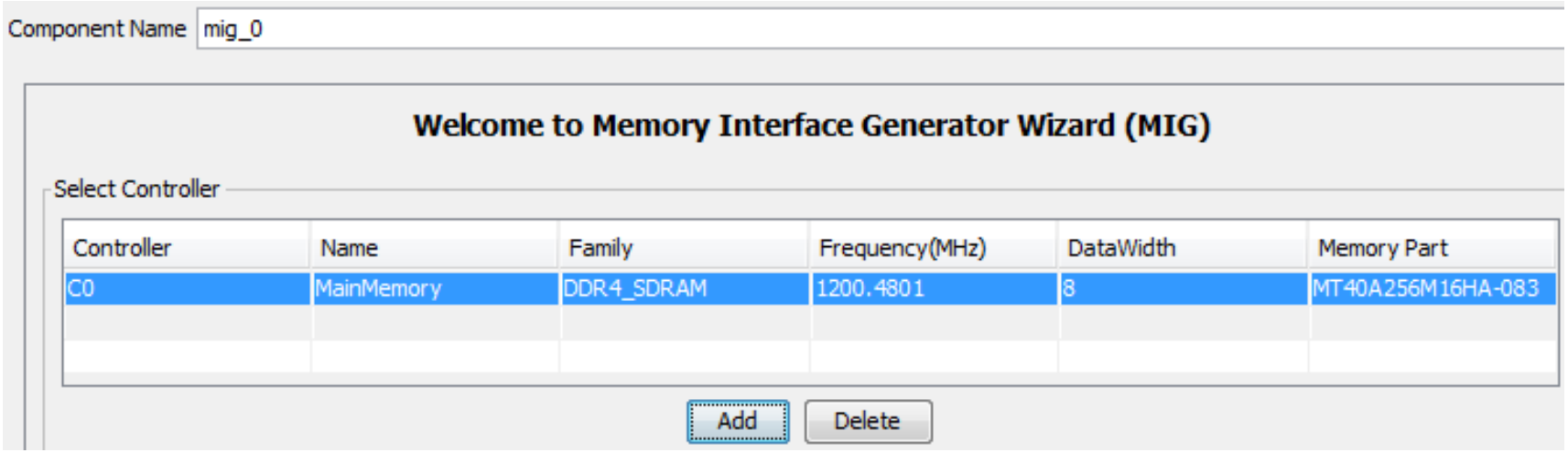
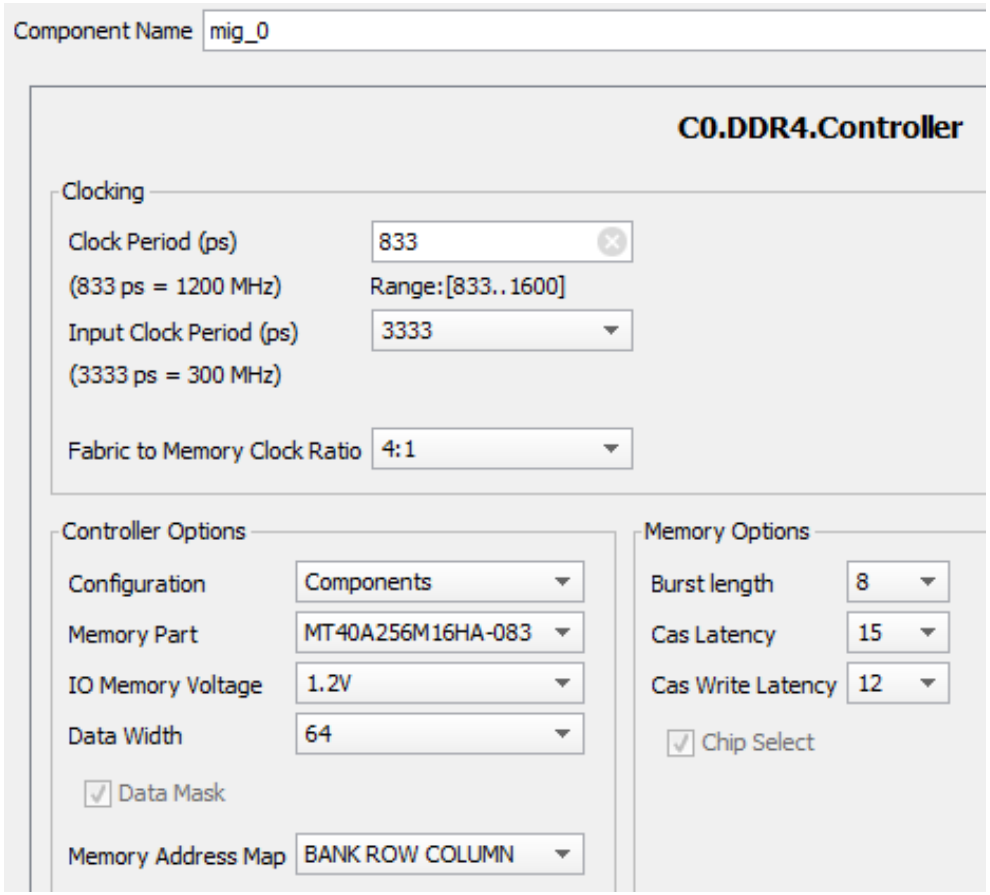
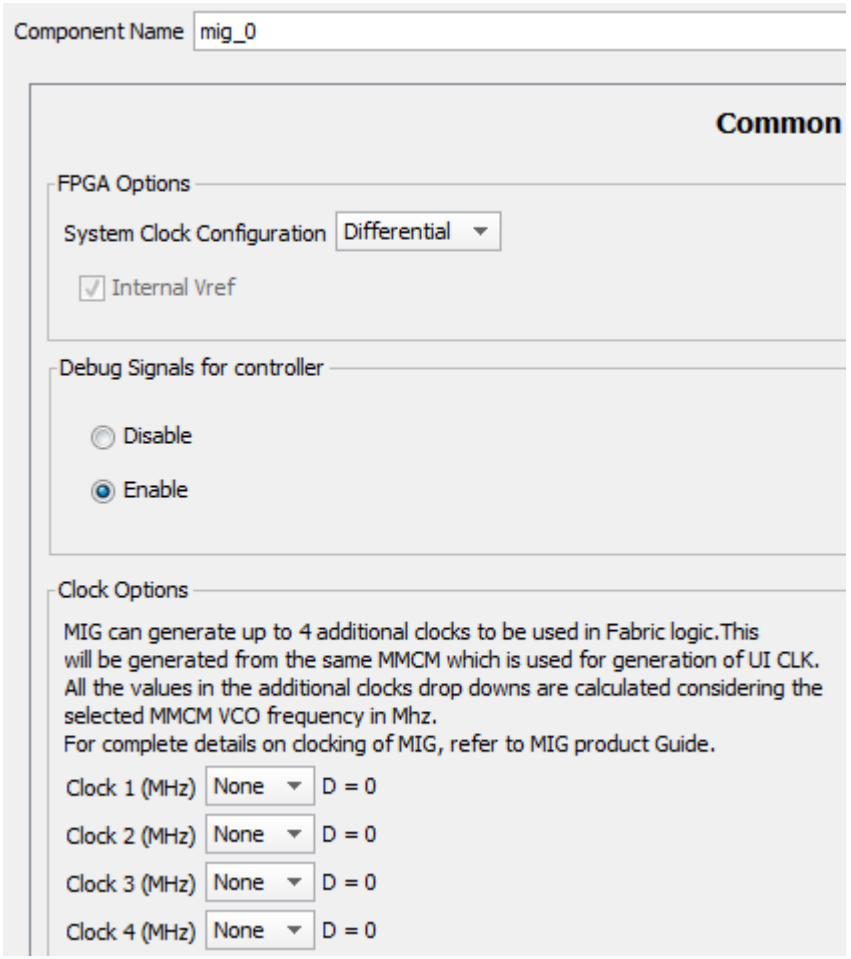




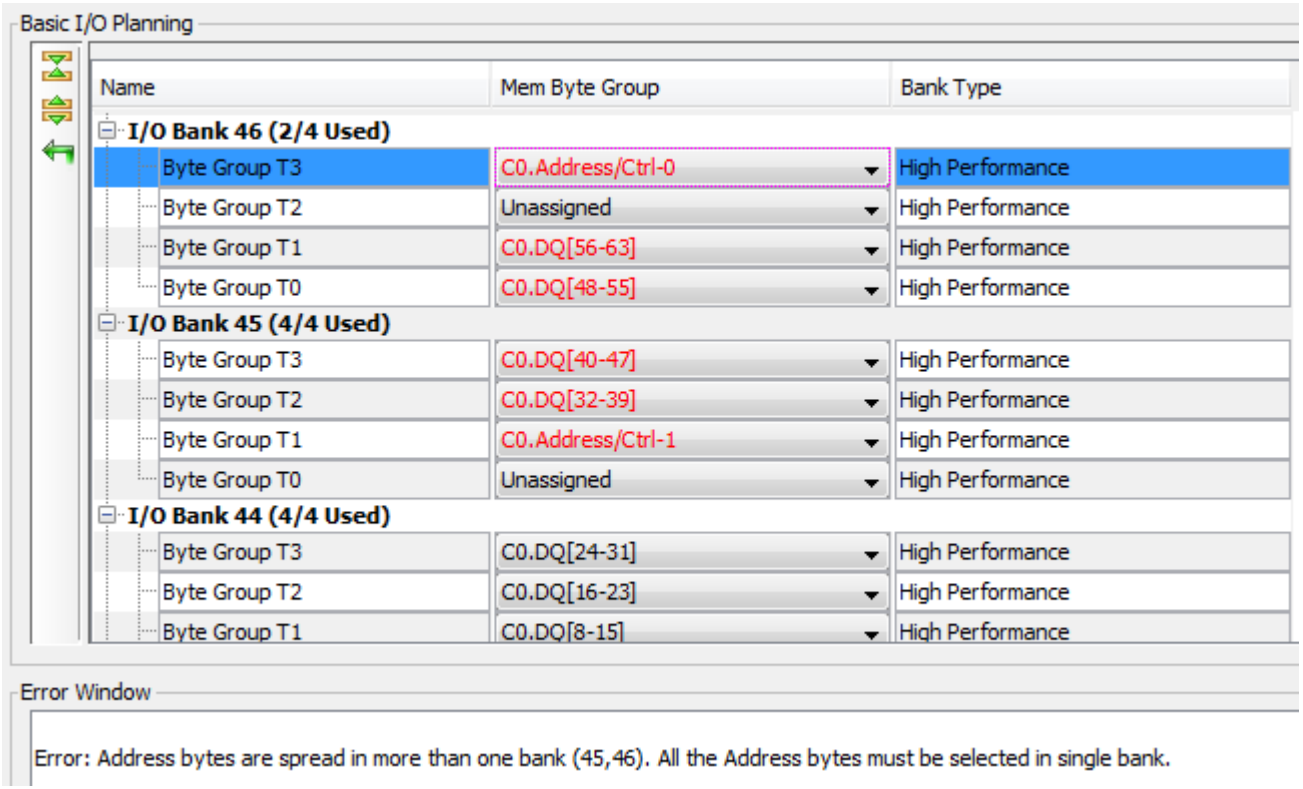


MIG Demo – Set Parameters





MIG Demo – Floorplan



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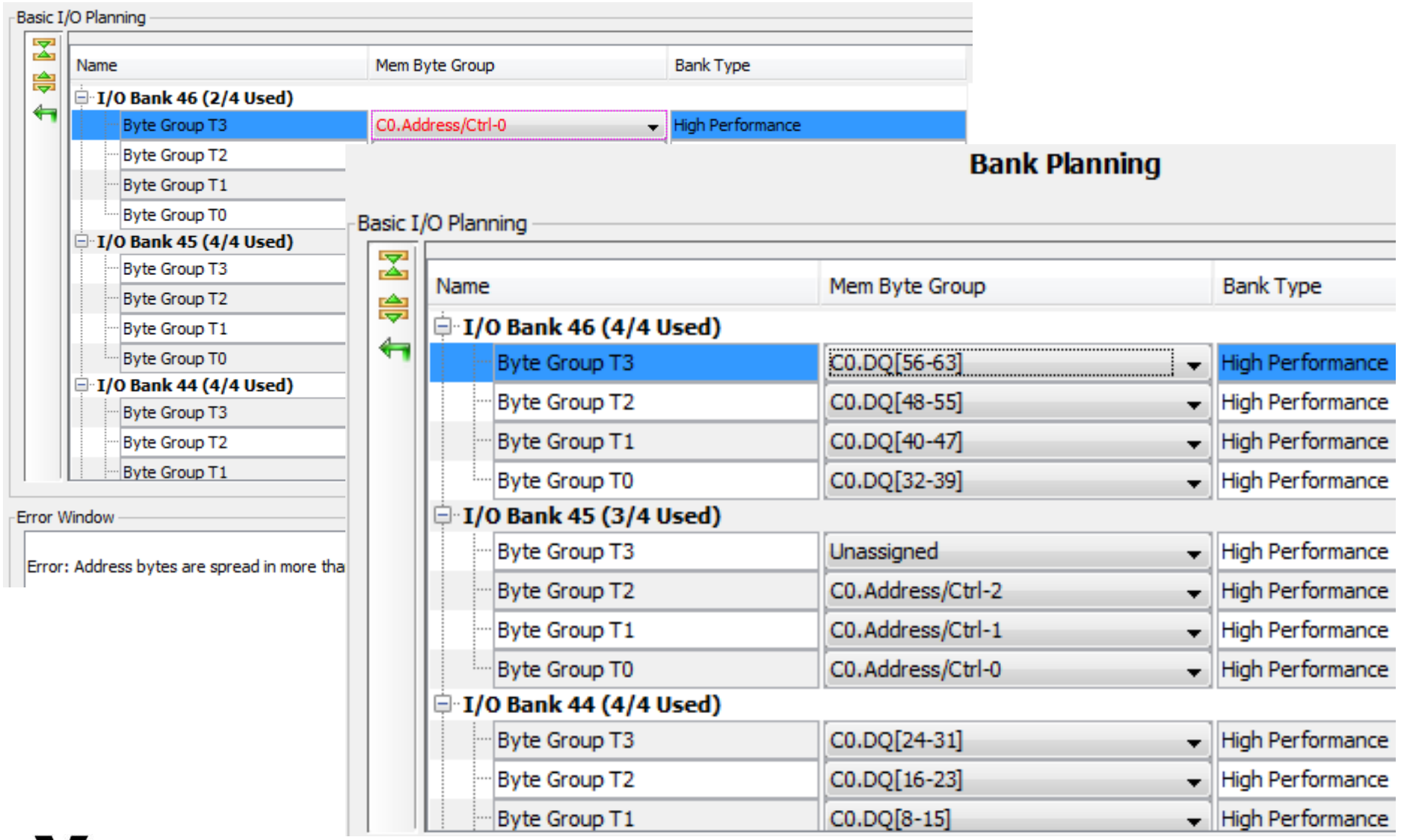
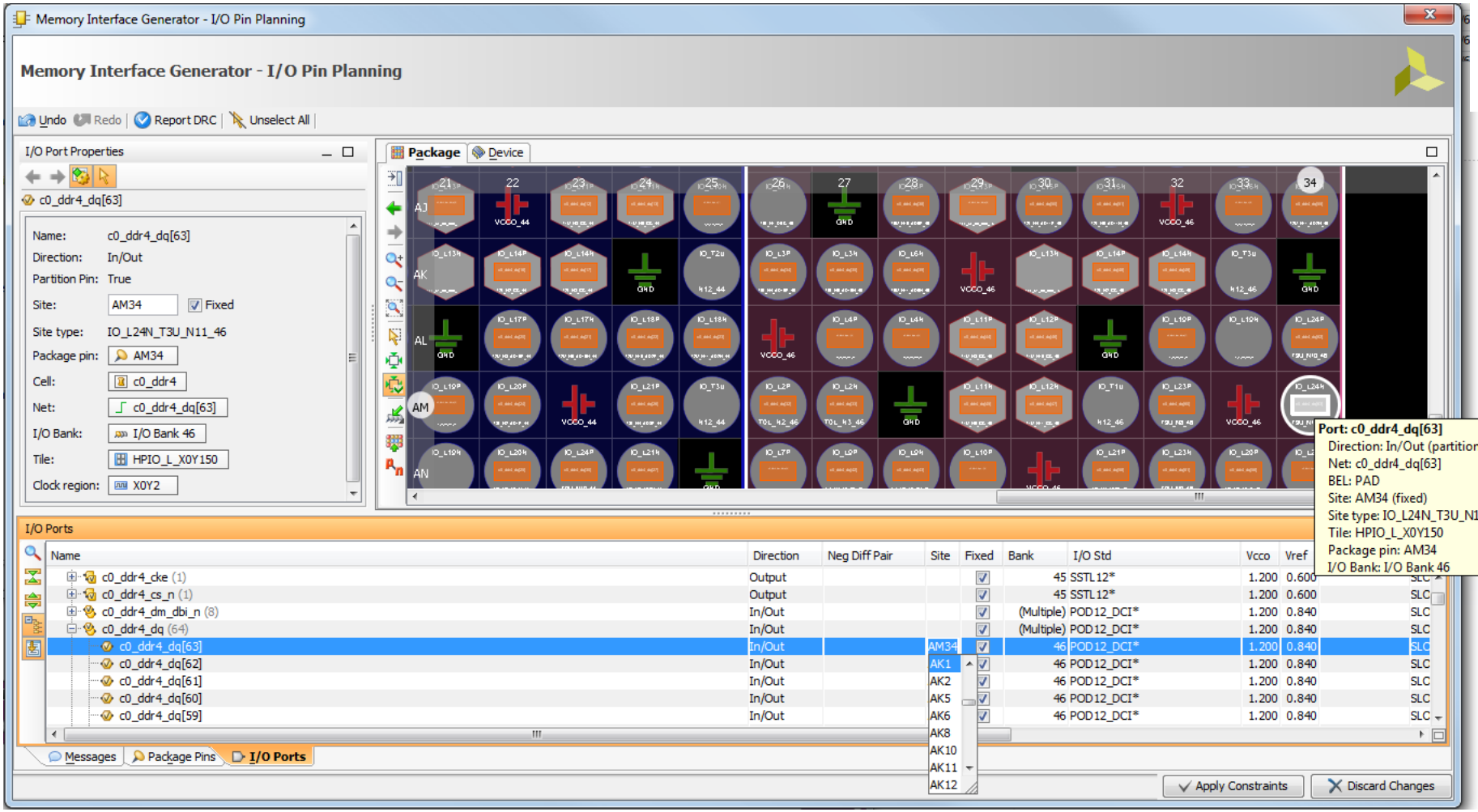


MIG Demo – Run MIG I/O Pin Planner



MIG Demo – Summary

MIG Configuration Summary

FPGA Options

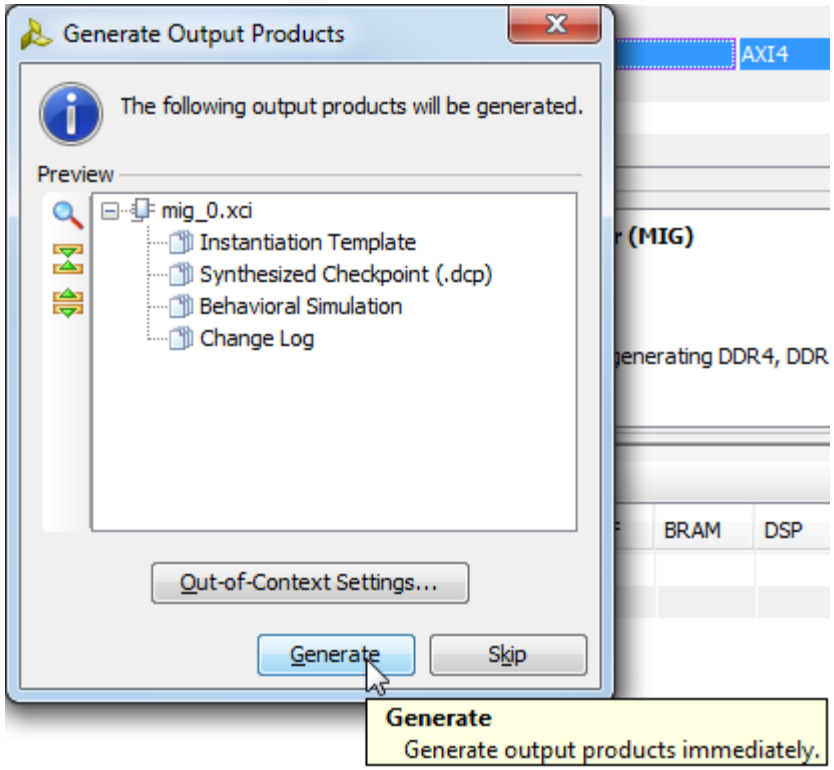
System Clock Type:	Differential
Reference Clock Type:	Differential
Internal Vref:	true

Controller Options

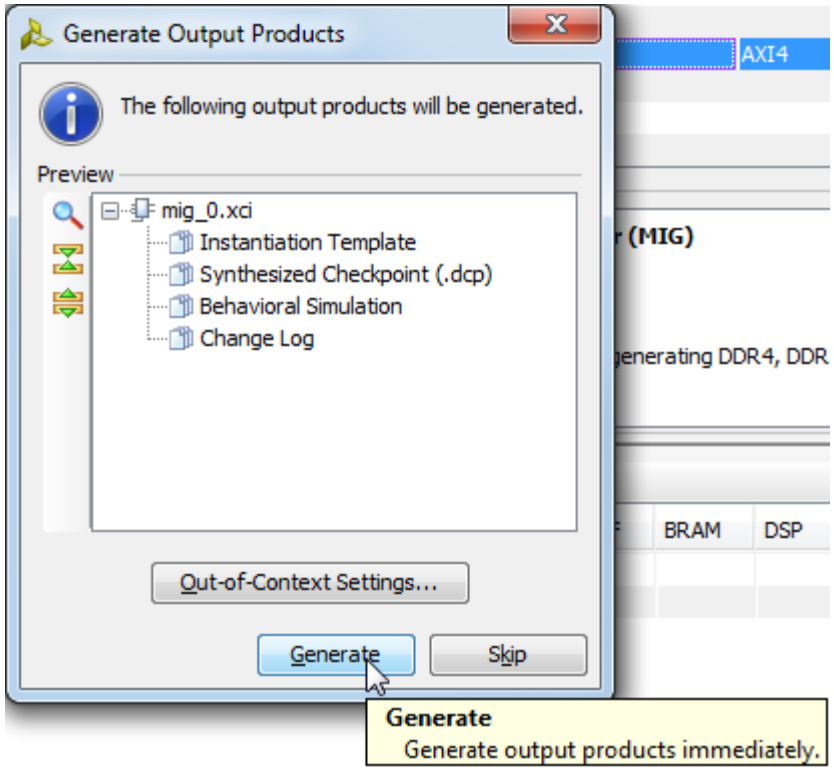
Controller 0

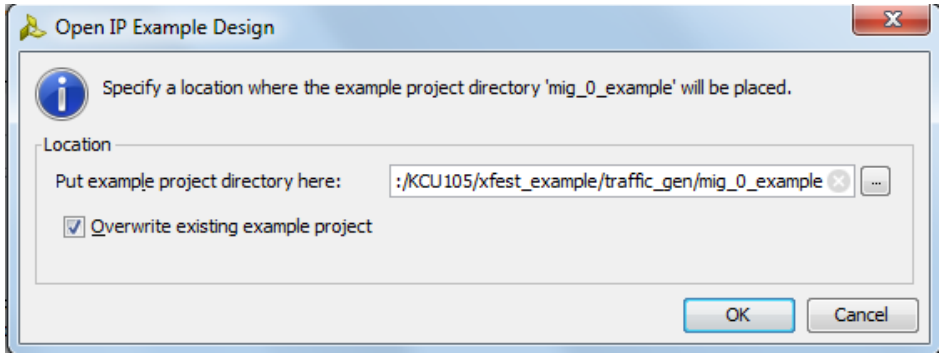
Memory:	DDR4_SDRAM
Design Clock Frequency:	(833 ps = 1200 MHz)
Phy Controller to Clock Ratio:	4:1
Input Clock Period:	(3333 ps = 300 MHz)
Memory Type:	Components
Memory Part:	MT40A256M16HA-083
Data Width:	64
Data Mask:	Enabled
Memory Address Map	BANK ROW COLUMN
Debug Signal for Memory Controller:	Enabled

MIG Demo – Generate Controller and Example

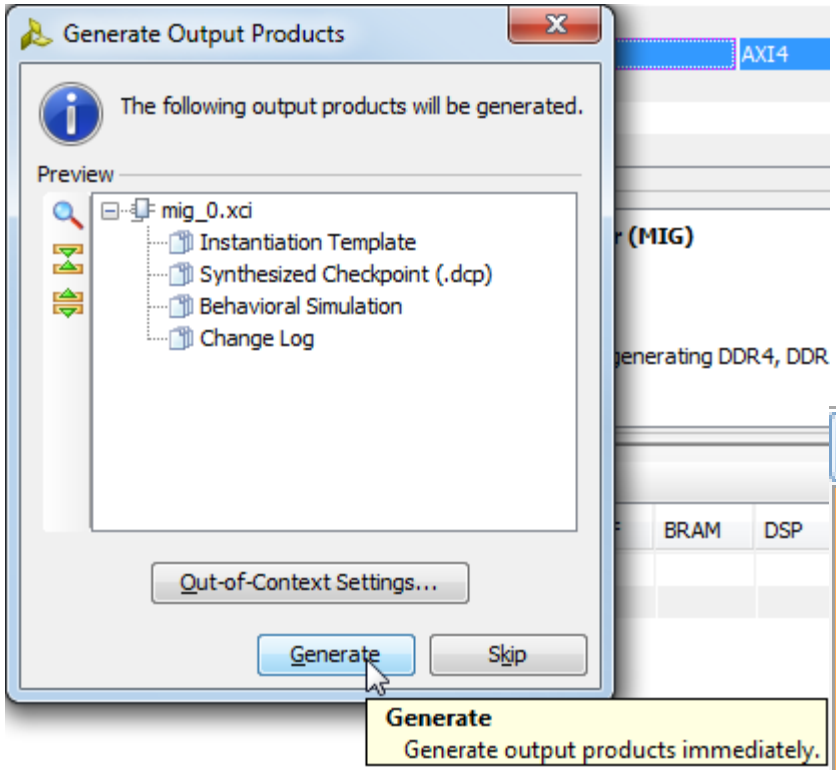


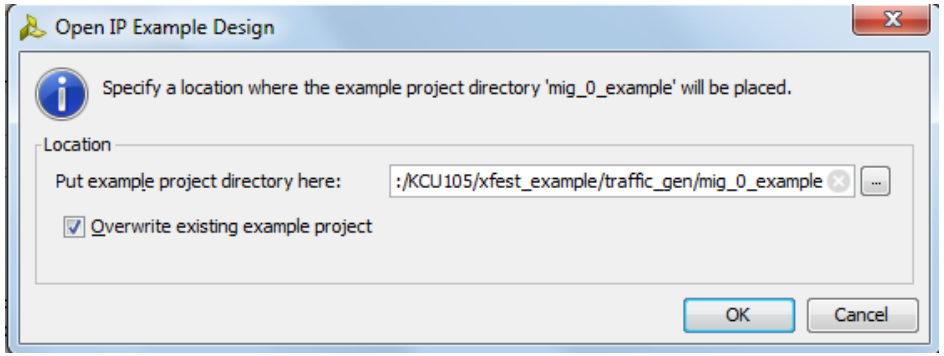
MIG Demo – Generate Controller and Example

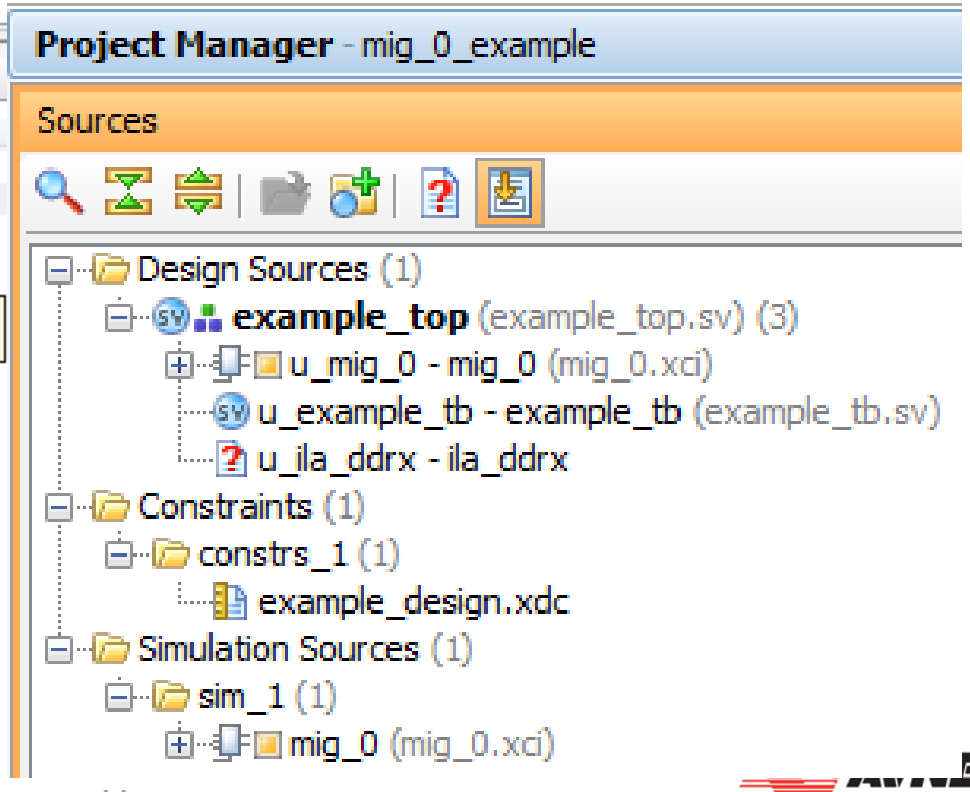




MIG Demo – Generate Controller and Example





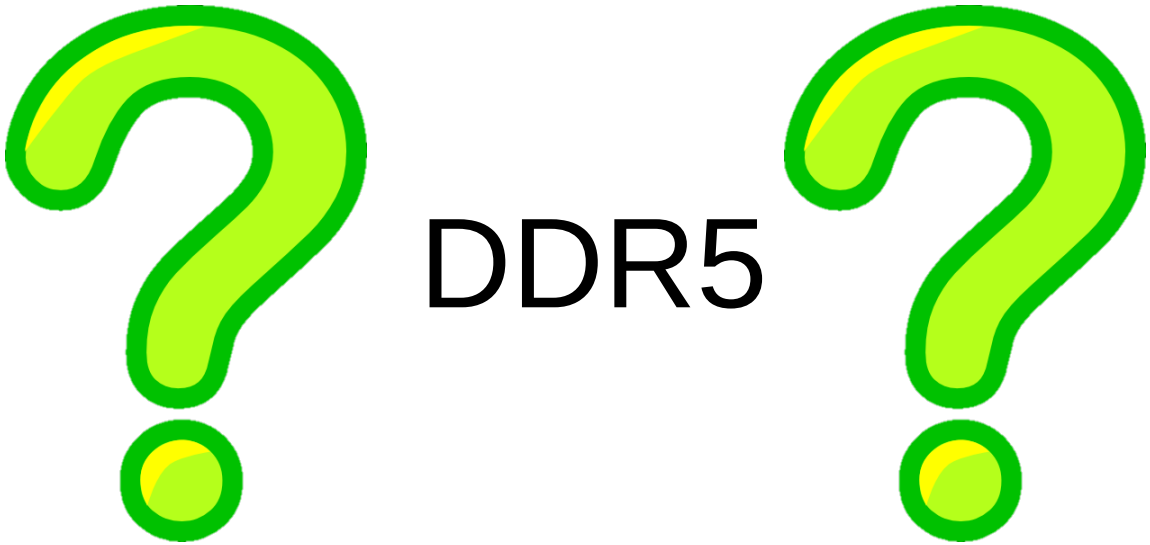


MIG Demo Summary

- **Build custom memory interfaces with MIG**
- **Generate the memory interface and controller quickly and easily**
- **Accelerate design productivity with MIG and the hardware-verified IP library**

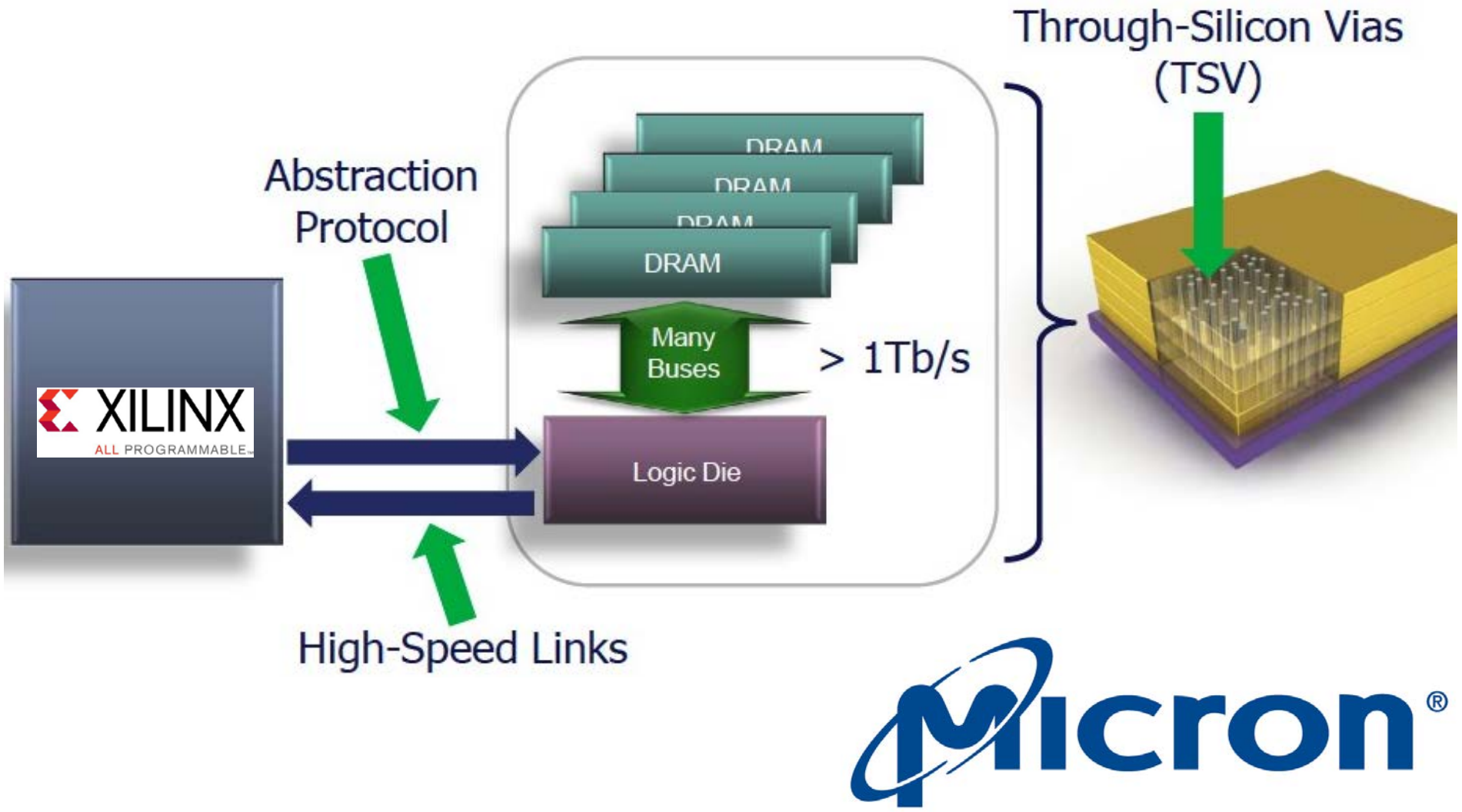
Next Generation Memory

What comes after DDR4?



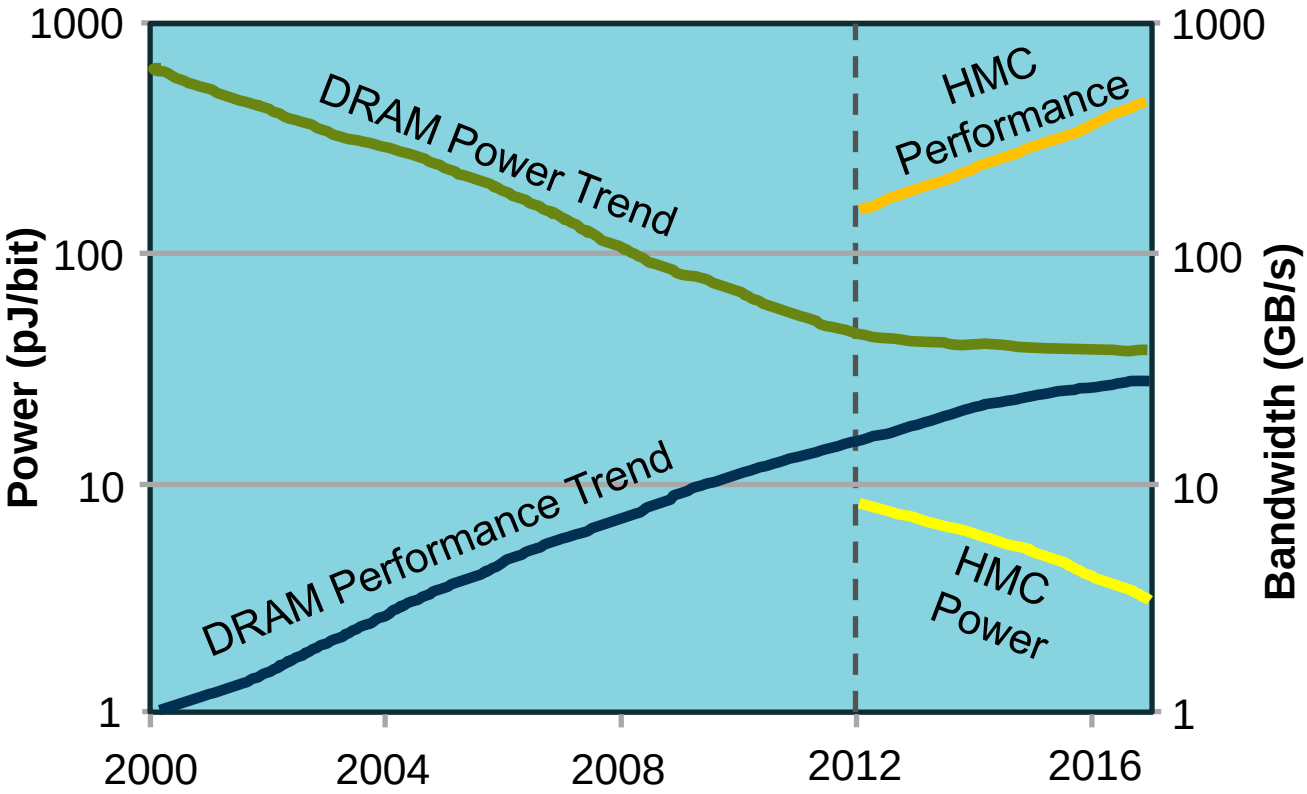
Hybrid Memory Cube

Hybrid Memory Cube (HMC)



HMC Advantages over DRAM

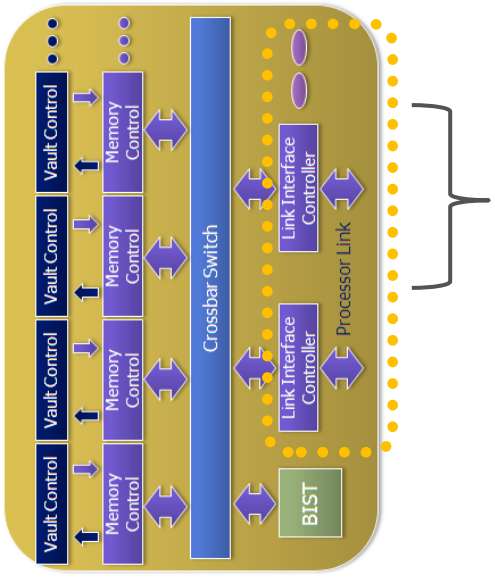
- **Reduced power**
  - Up to 70% less energy per bit
- **Fewer pins**
  - Up to 85% less pins
- **Reduced footprint**
  - 90% less space than today's RDIMM
- **Increased Bandwidth**
  - 15x the performance



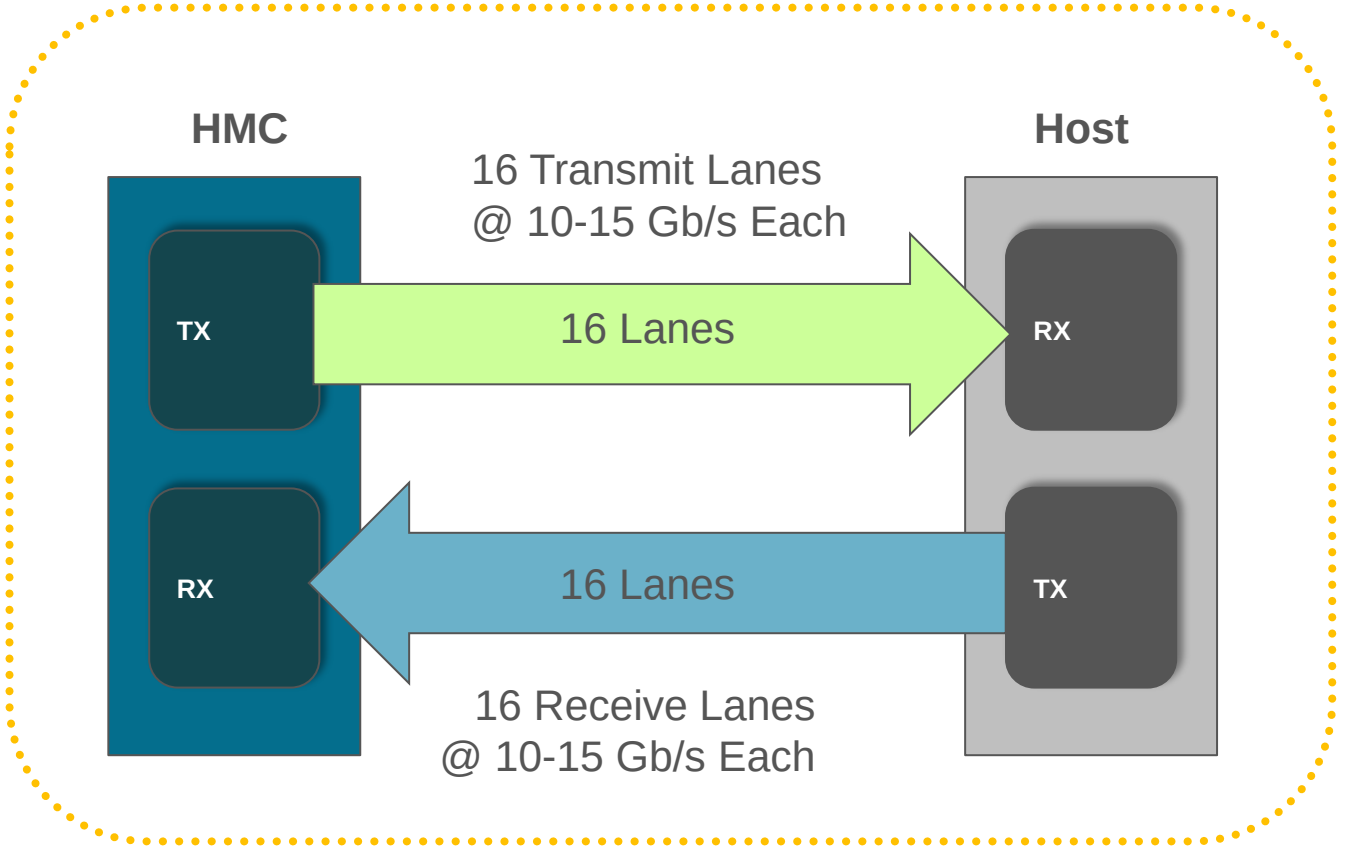
*Compared to DDR3-1333

Link Controller Interface

HMC
Logic Base



Each HMC device has four **Links**

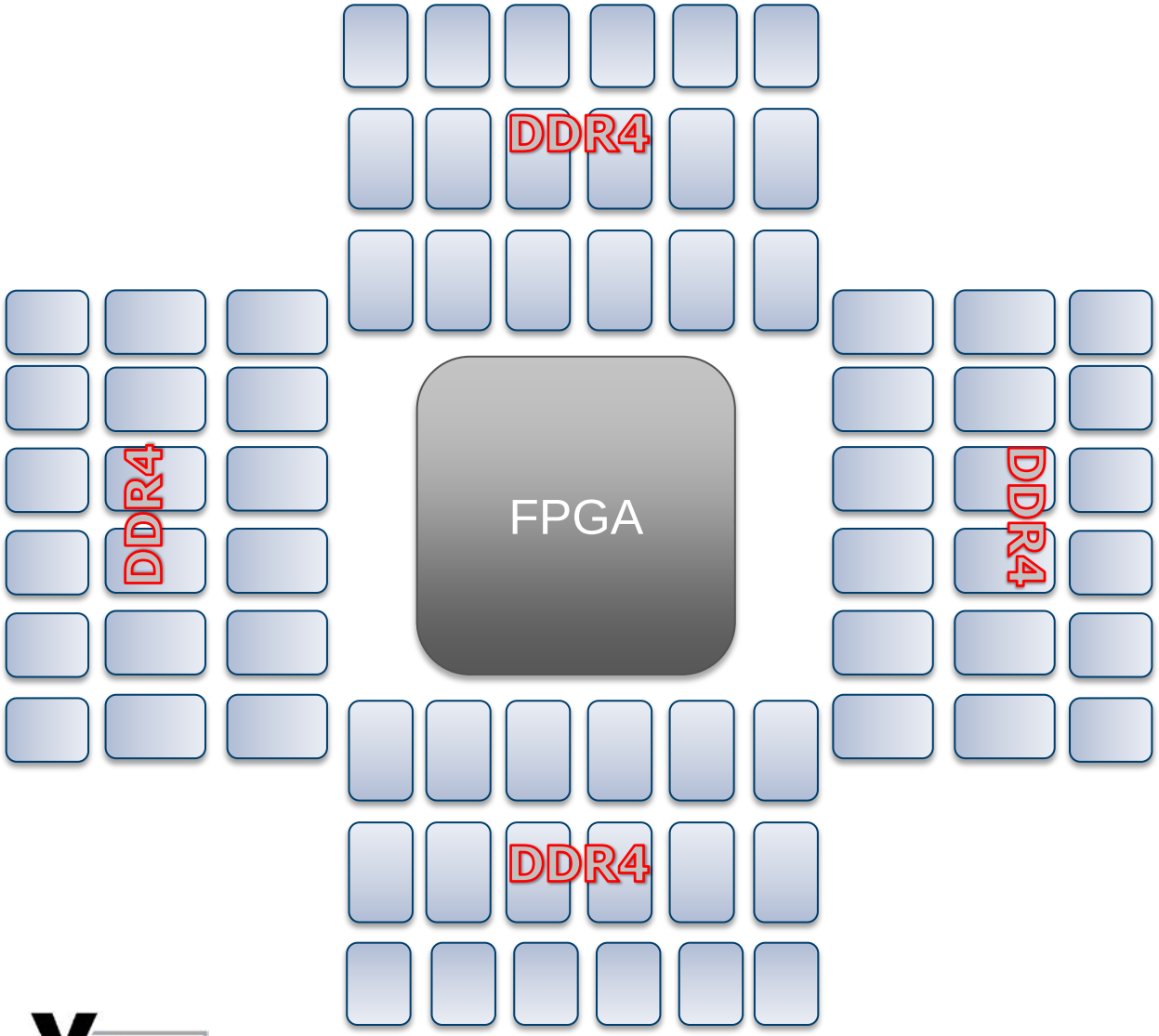


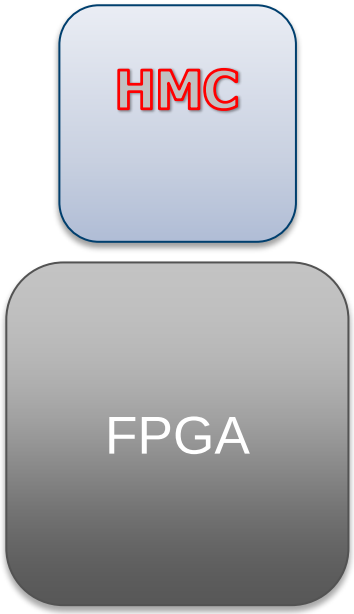
Each **Link** has 32 differential **Lanes**

400 Gbps Packet Buffer Example (with ECC)

Parameter	DDR4-2400	HMC 12.5G 4 Links	HMC Advantage
Number of Memory Devices	48 – x16 24 – x4	1	72 to 1
Total Number of Pins	1,896	276	85% fewer pins
Host PHY + Memory Power	49 W	32 W	35% lower power
Memory Surface Area	8,532 mm^2	961 mm^2	89% smaller footprint
Host PHY Silicon Area	1.75x	1x	75% smaller host PHY

400 Gbps Packet Buffer Comparison





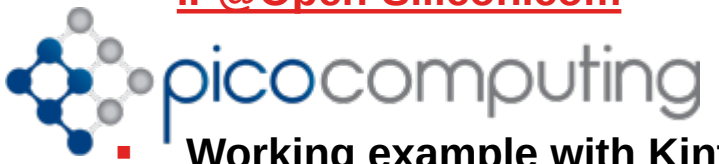
All devices drawn to scale

IP Requirements

- **Virtex-7, Kintex UltraScale, or Virtex UltraScale**
- **10, 12.5, or 15 Gbps SERDES**
  - 16 SERDES for full Link (16 Tx / 16 Rx)
- **IP licensing**
  - Includes first year of maintenance and support
  - License fee per project

Configuration	Price
Half-width 10G	$40,000
Half-width 12.5G	$45,000
Half-width 15G	$50,000
Full-width 10G	$50,000
Full-width 12.5G	$60,000
Full-width 15G	$70,000

- **Working example with Virtex-7**
- **Full-width Link (32 lanes) takes ~50K LUTs**
- **IP@Open-Silicon.com**



- **Working example with Kintex UltraScale – Pico EX-850 Board**
- **Full-width Link (32 lanes) takes ~35K LUTs**
- **Contact@picocomputing.com**
- **Other pricing upon request**

Configuration	Price
Full-width 10G	$65,000

Next Steps

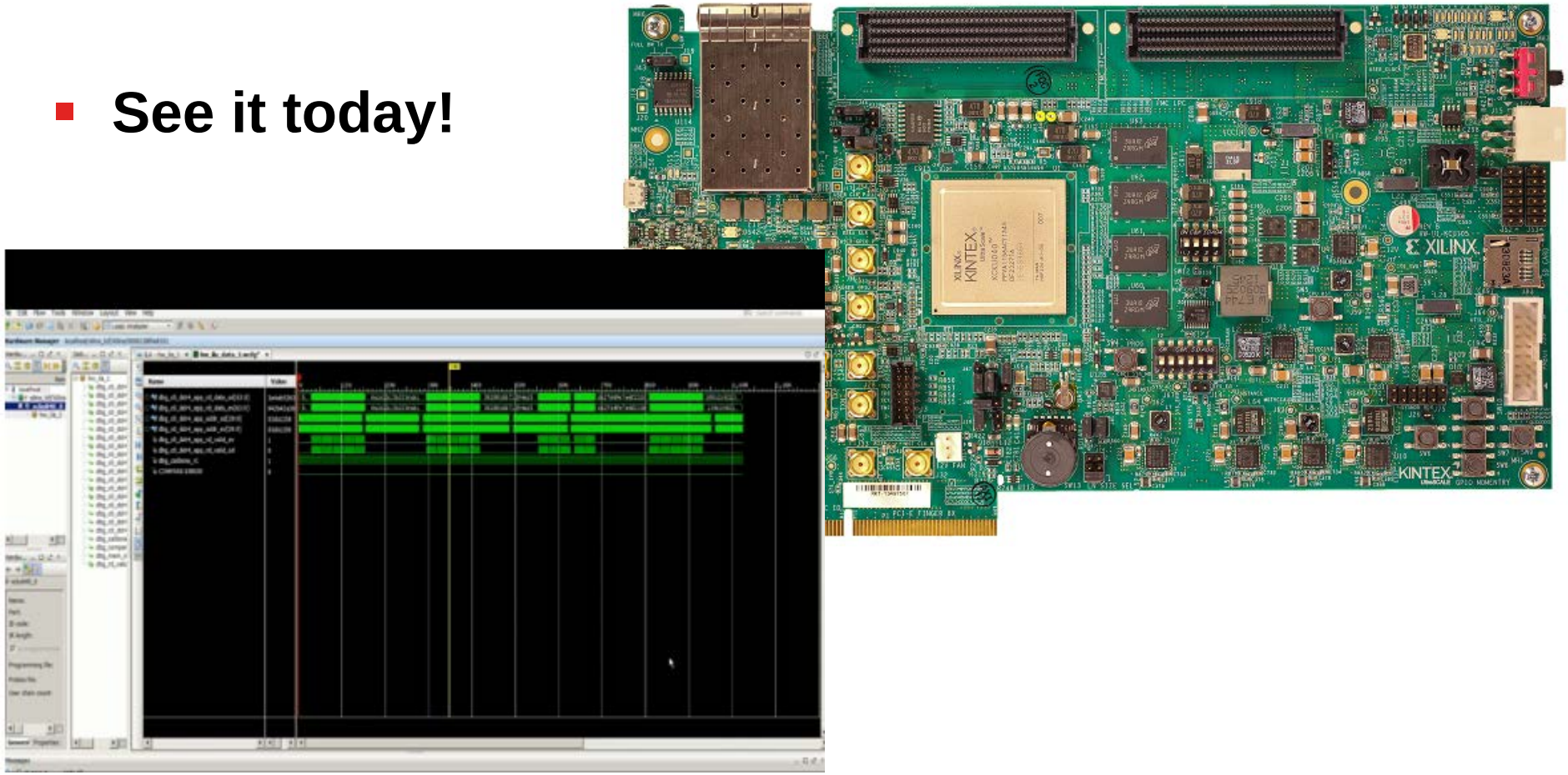
What Have We Learned?

- **Major differences between DDR4 and DDR3**
- **Memories supported with UltraScale**
- **How to design an UltraScale DDR4 memory controller using MIG**
- **Preview next generation memory interfaces**

How can you learn more?

See UltraScale and DDR4 Running at 2400 Mbps!

- **KCU105 / DDR4-2400 demo on the Xilinx table**
- **See it today!**



Buy the KCU105 Evaluation Kit

www.xilinx.com/KCU105

Cables and Power

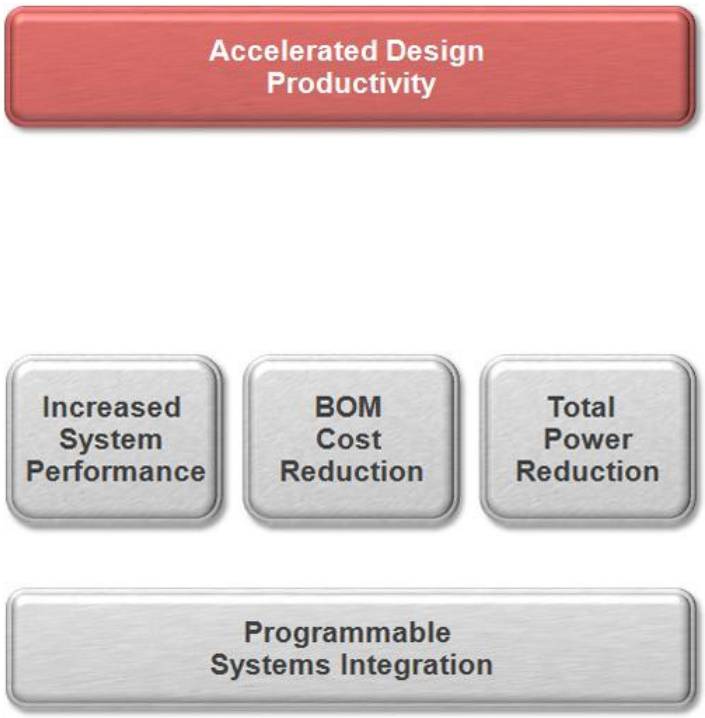
Reference Designs and Docs

Kintex UltraScale KCU105 Evaluation Board

Vivado® Design Suite Development Tools

Ordering Information	
Part Number:	EK-U1-KCU105-G
Price:	TBA
Shipping:	Q1 2015

Xilinx Two-day Course:
How to Design a High-Speed Memory Interface



- **Build designs faster using memory interfaces**
- **Gain knowledge, confidence, and experience to build memory interface designs**
- **Learn how Xilinx hardware and software provides single device solutions, simplifying the bill of materials (BOM), and reducing cost**
- **Use programmable logic to customize the memory interface to your system needs**

ARTIX-7 KINTEX-7 VIRTEX-7 ZYNQ VIVADO

www.xilinx.com/training/connectivity/designing-high-speed-memory-interfaces.htm

Or search the web for "*Xilinx Memory Interface Course*"

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www.xfest2014.com

- **PDFs of all presentations**
- **Course forums**

Reference Information on UltraScale DDR4

- http://www.micron.com/products/dram/ddr4-sdram
- http://www.micron.com/products/support/power-calc
- http://www.micron.com/products/dram/ddr3-to-ddr4
- www.xilinx.com/ultrascale
- http://www.xilinx.com/products/design_tools/logic_design/xpe.htm
- www.xilinx.com/kcu105
- WP454 *High-Performance, Lower-Power Memory Interfaces with UltraScale Architecture FPGAs*
- PG150 *LogiCORE IP UltraScale Architecture-Based FPGAs Memory Interface Solutions*
- UG583 *UltraScale Architecture PCB Design and Pin Planning*
- UG917 *KCU105 Board User Guide*
- http://www.xilinx.com/products/technology/memory-interfacing/index.htm#uniquePlayer1
- http://www.xilinx.com/products/technology/memory-interfacing/index.htm#uniquePlayer2
- http://www.xilinx.com/training/ultrascale/designing-a-memory-interface-and-controller-with-vivado-mig-for-ultrascale.htm
- www.xilinx.com/training/connectivity/designing-high-speed-memory-interfaces.htm
- http://www.xilinx.com/support/answers/59625.html

Reference Information on UltraScale HMC

- http://www.micron.com/products/hybrid-memory-cube
- Xcell Journal, Issue 88 *Goodbye DDR, Hello Serial Memory*
- http://picocomputing.com/products/hybrid-memory-cube-hmc-controller-ip/
- http://forums.xilinx.com/t5/Xcell-Daily-Blog/HMC-demo-shows-15Gbps-operation-per-link-at-last-month-s/ba-p/488174
- http://forums.xilinx.com/t5/Xcell-Daily-Blog/Hybrid-Memory-Cube-HMC-controller-and-interface-IP-rips-along-at/ba-p/480012
- http://www.hotchips.org/wp-content/uploads/hc_archives/hc23/HC23.18.3-memory-FPGA/HC23.18.320-HybridCube-Pawlowski-Micron.pdf


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You
Maake
Asante
Dhanyavadagalu
Shukria
Kiitos
Vinaka
köszönöm
спасибо
Dankscheen
감사합니다
Kam Sah Hammida
شكرا
Manana
Dankon
Matondo
Dank Je
Maururu
Biyan
Terima Kasih
Taiku
Tack
Blagodaram
Ngiyabonga
Dziekuje
Chokrane
Diolch i Chi
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cảm ơn bạn
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Ua Tsaug Rau Koj
Bedankt
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ありがとう
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Merci
Go Raibh Maith Agat
Eskerrik Asko
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谢
ขอขอบคุณคุณ
Salamat
Najis Tuke