



PRESENTED BY



Bryan Fletcher

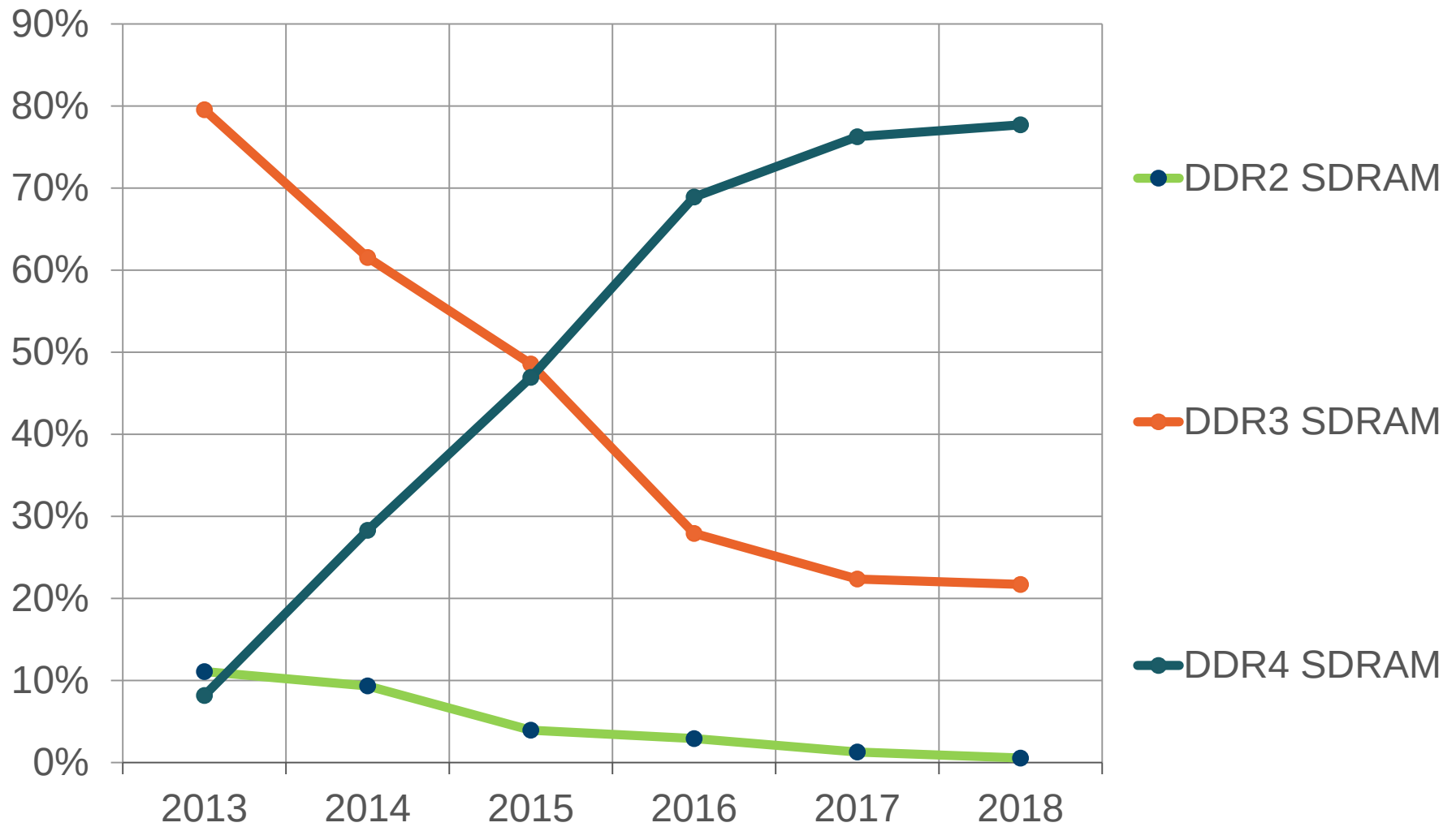
UltraScale™ Memory Interfaces

Memory Interface Criteria

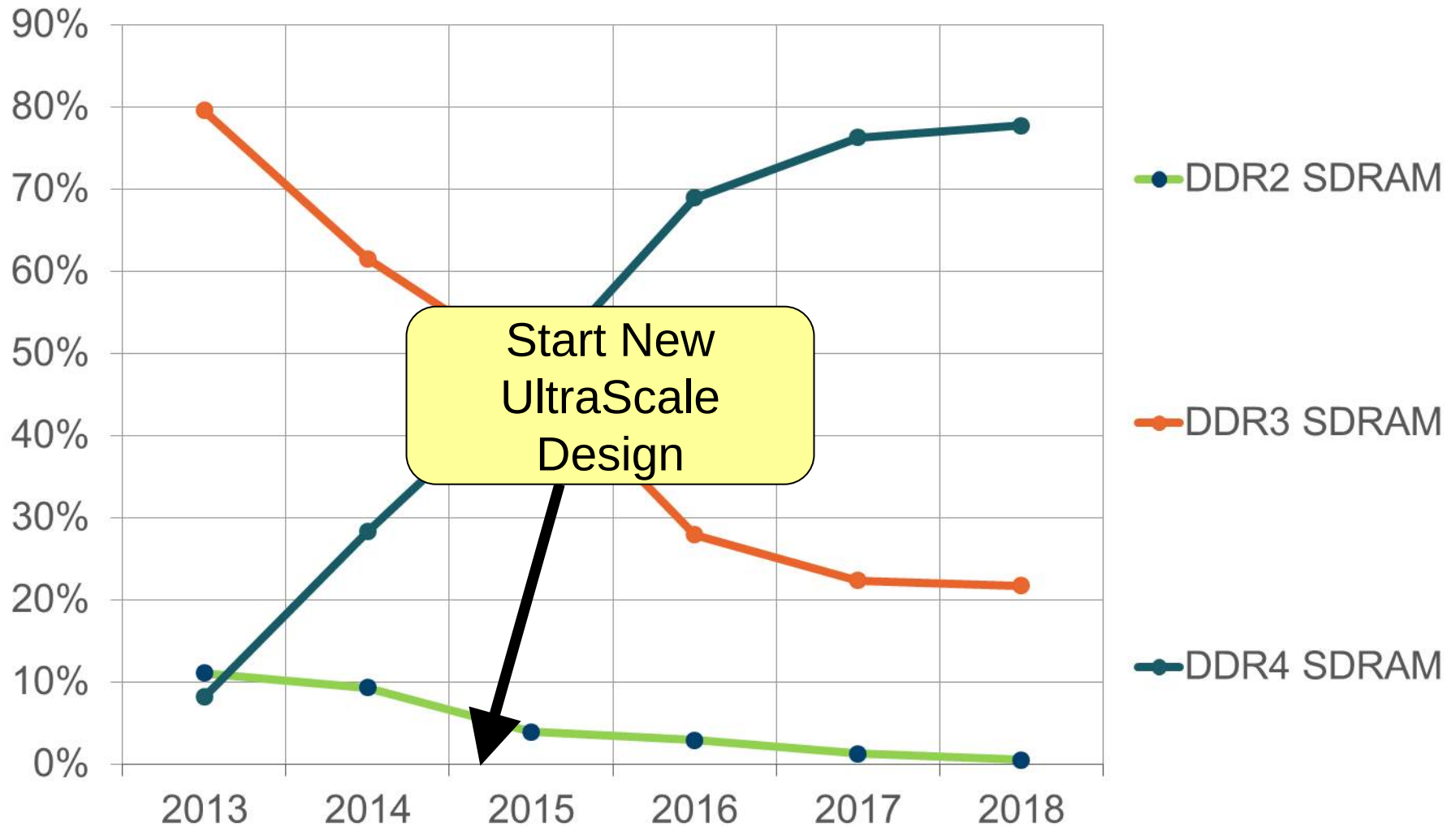
- **System designers prefer memory interfaces with**
 - Less **P**ower
 - More **P**erformance
 - Lowest **P**rice per bit

- **DDR4 delivers in all three areas with UltraScale™ (compared to DDR3)**

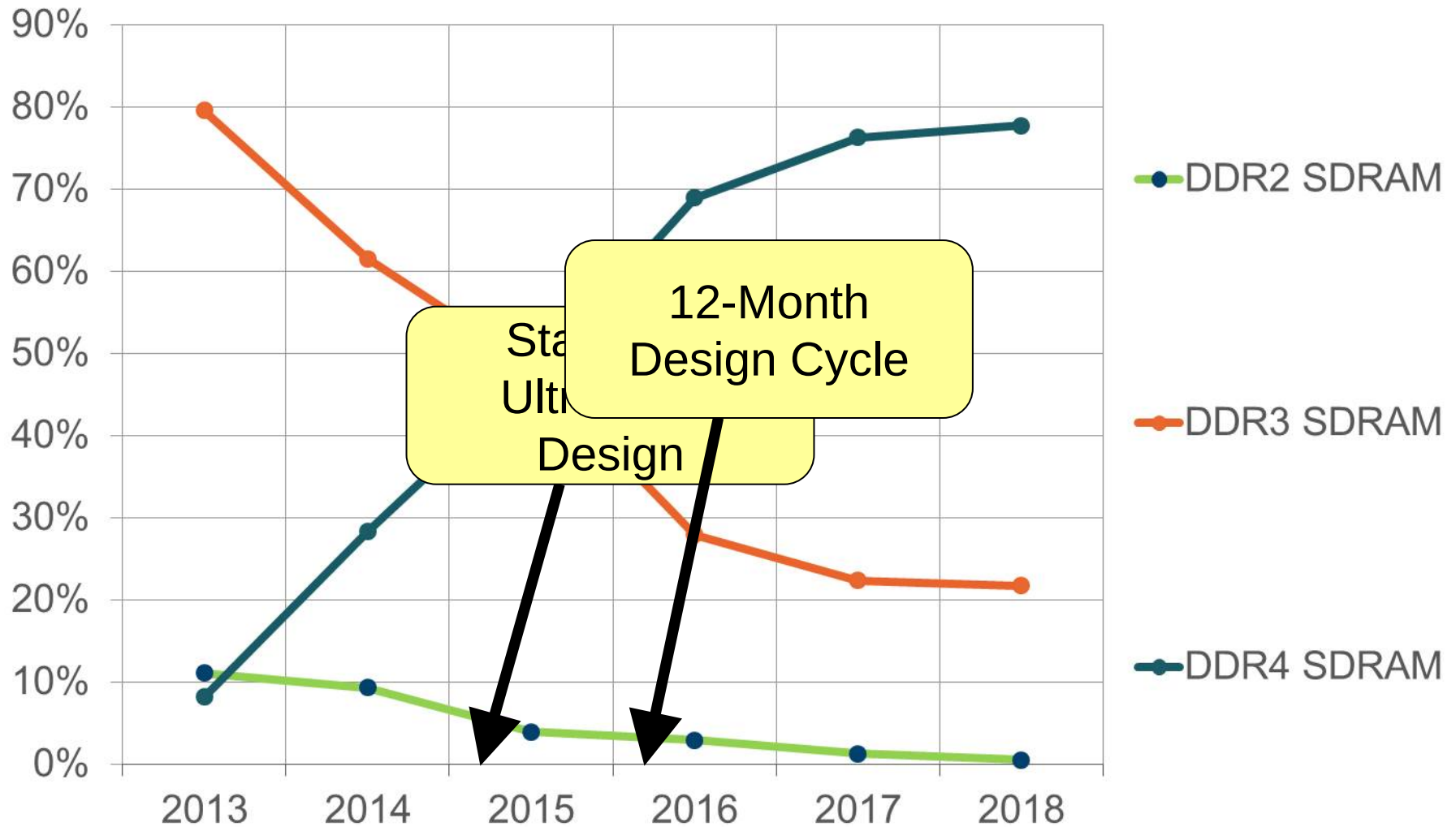
DDR SDRAM Market Share



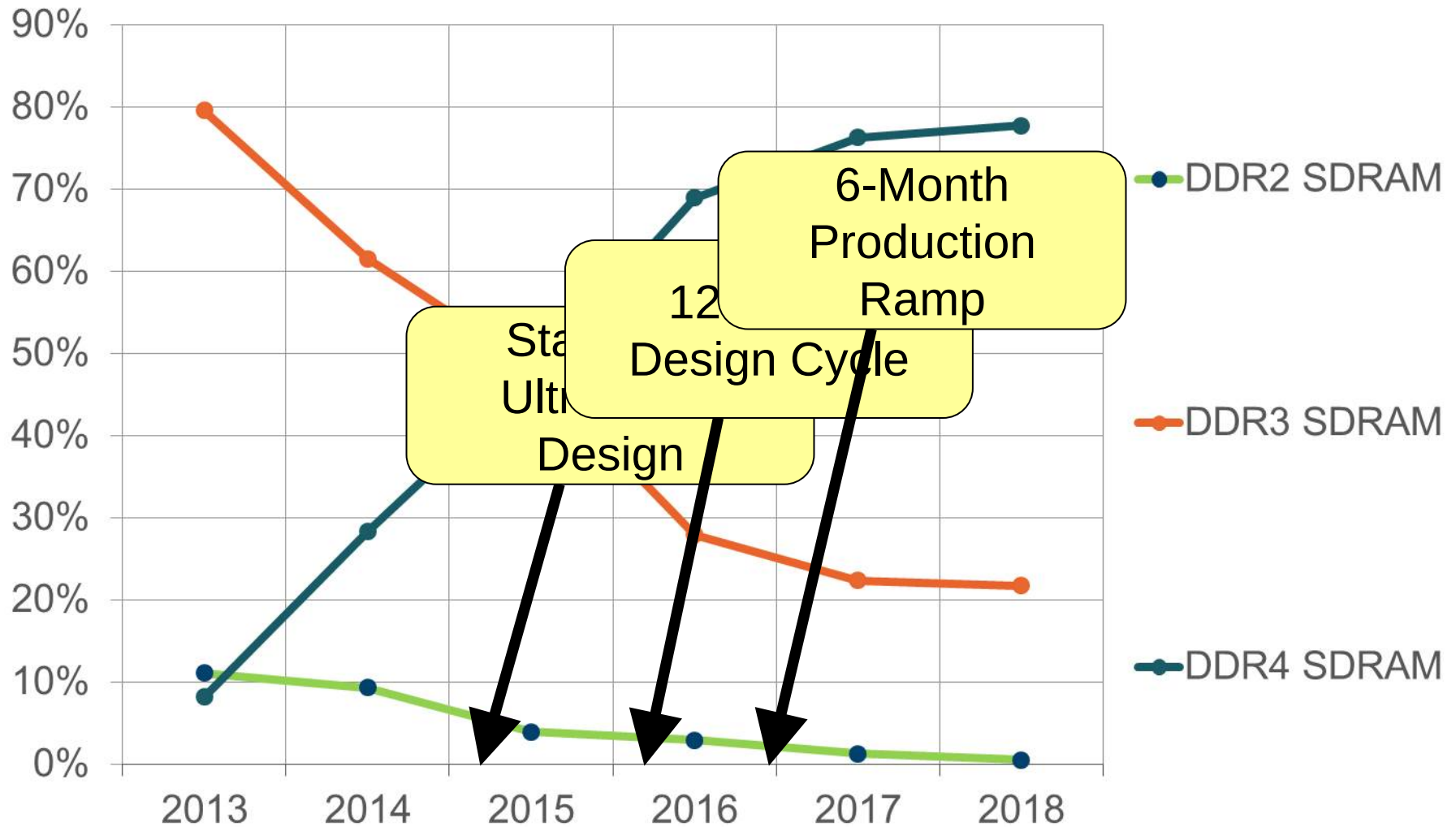
Design Timeline



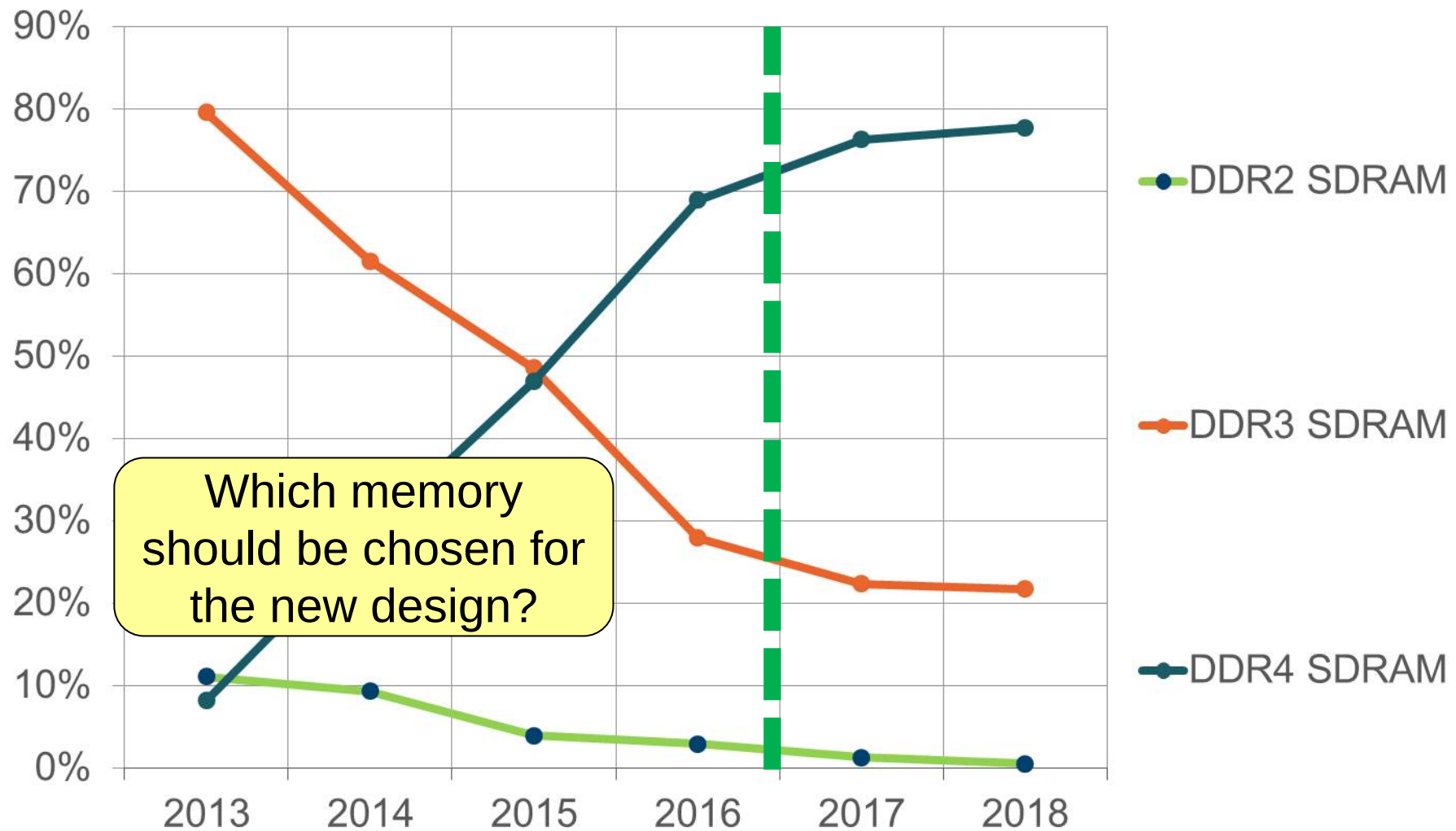
Design Timeline



Design Timeline



Design Timeline



Objectives

- Explore major differences between DDR4 and DDR3
- Know which memories are supported with UltraScale
- See how to start a DDR4 memory controller design in UltraScale using MIG
- Preview next generation memory interfaces

Agenda

- **Technology differences: DDR4 vs. DDR3**
- **UltraScale memory interface features**
- **System design-in considerations for DDR4 with UltraScale**
- **Creating an UltraScale DDR4 memory controller**
- **Next generation memory**

Technology Differences: DDR4 vs. DDR3

Remember Slide 2?

DDR4 Advantages in

- **Power**
- **Performance**
- **Price**

Memory Interface Criteria

- System designers prefer memory interfaces with
 - Less **P**ower
 - More **P**erformance
 - Lowest **P**rice per bit
- DDR4 delivers in all three areas with UltraScale™ (compared to DDR3)



2



DDR3 vs. DDR4: Voltage and Power

Features	DDR3 /L	DDR4	DDR4 Improvements
V_{DD}/V_{DDQ}	1.5V/1.35V	1.2V	25% reduction to DDR3
V_{PP}	internal word-line charge pumps	2.5V	More cost-effective and allows lower $V_{DD/Q}$
V_{TT}	$\frac{1}{2} V_{DD}/V_{DDQ}$ sink/source	$\frac{1}{2} V_{DD}/V_{DDQ}$ sink/source	25% reduction to DDR3
V_{REF} Inputs	$\frac{1}{2} V_{DD}/V_{DDQ}$ DQ and CA	$\frac{1}{2} V_{DD}/V_{DDQ}$ CA only	V_{REFDQ} is internal
DQ Termination	SSTL	Pseudo-Open Drain (POD)	Reduces termination current
Example: Power (IDD7)	339mW (DDR3L, 30nm, 4Gb, 1866MT/s)	247mW (DDR4, 30nm, 4Gb, 1866MT/s)	27% less power

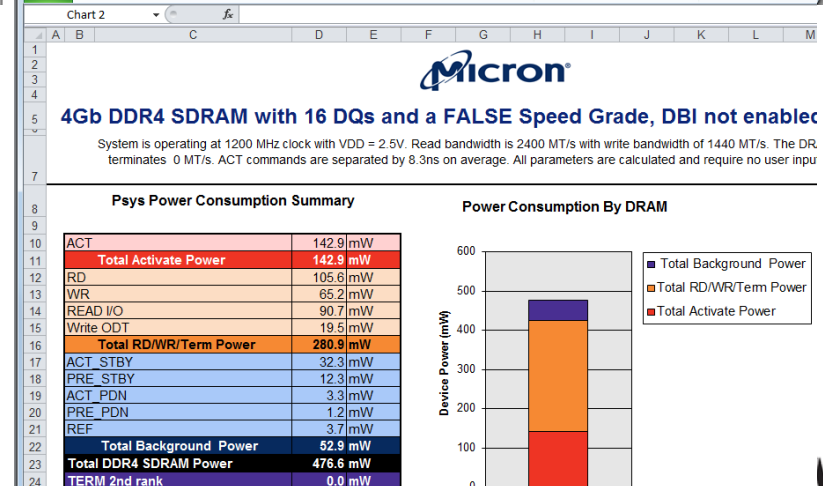
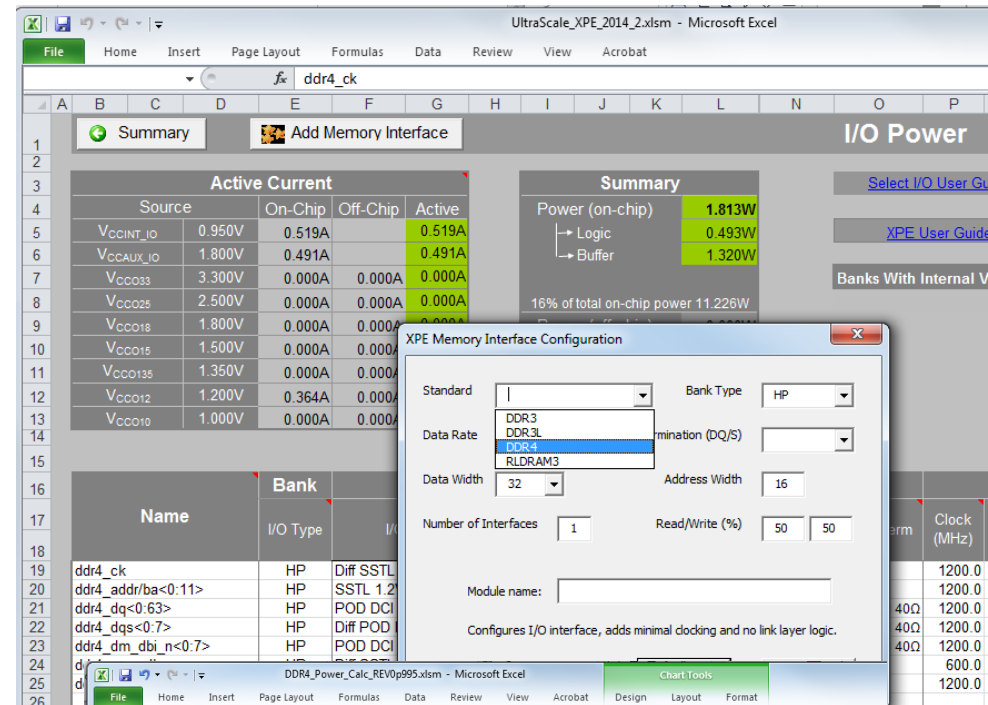
FPGA Power Savings

Interface	Rate/Width	IO/PHY Power	% Savings
DDR3, 7-Series	1866 Mb/s, 32-bit	1.41 W	-
DDR4, UltraScale	1866 Mb/s, 32-bit	0.94 W	33%
DDR4, UltraScale	2400 Mb/s, 32-bit	1.10 W	22%

DDR4 Power Circuit Design – $V_{DD/Q}$ and V_{PP}

- V_{DD} and $V_{DDQ} = 1.2 \text{ V}$
 - +/- 5% tolerance
 - May share a single supply
 - Also may share supply with FPGA V_{CCO}
 - Switching regulators are a good choice
 - Single shared supply may require multiple amps
 - Use **Power Calculators** to estimate

- $V_{PP} = 2.5 \text{ V}$
 - +/-10% tolerance
 - Check DDR4 datasheet for current requirements
 - ~30 mA for one 4Gb device



DDR4 Power Circuit Design – V_{TT} and V_{REF}

- **V_{TT} and V_{REF} value are dictated by $V_{DD/Q}$**
 - Must be 50% of your $V_{DD/Q}$ voltage
 - V_{TT} must be sink/source
- **V_{TT} / V_{REF} dedicated termination regulators**
 - TPS5120x family from Texas Instruments
 - NCP51199 from OnSemi
 - MAX1510 from Maxim Integrated
- **V_{REF} alternatives**
 - Low noise linear regulators
 - Resistor divider as seen on Xilinx KCU105
 - Internal V_{REF} required for UltraScale
- **V_{TT} alternative**
 - Synchronous switching regulators able to sink current
 - Needs to accurately regulate to 50% of your $V_{DD/Q}$



ON Semiconductor®

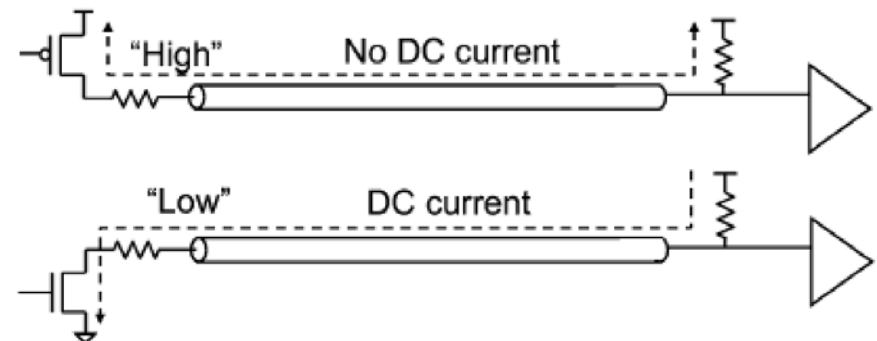


DDR4 Termination

- **Command/Address uses SSTL (same as DDR3)**
- **Data uses Pseudo Open Drain (POD) 1.2V**



- **POD driver has**
 - strong pull-down strength
 - weak pull-up strength
 - True open-drain has no pull-up strength
- **Requires external pull-up resistor to HIGH voltage**
 - In practice, this is accomplished internally
 - DCI in FPGA
 - ODT in DDR4 device
- **Advantage: no DC current during high drive**



DDR3 vs. DDR4: Performance in UltraScale

Features	DDR3 /L	DDR4	DDR4 Improvements
Data rate (Mb/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, 2667, 3200	50% faster

DDR3 vs. DDR4: Performance in UltraScale

Features	DDR3 /L	DDR4	DDR4 Improvements
Data rate (Mb/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, 2667 3200	13% 50% faster

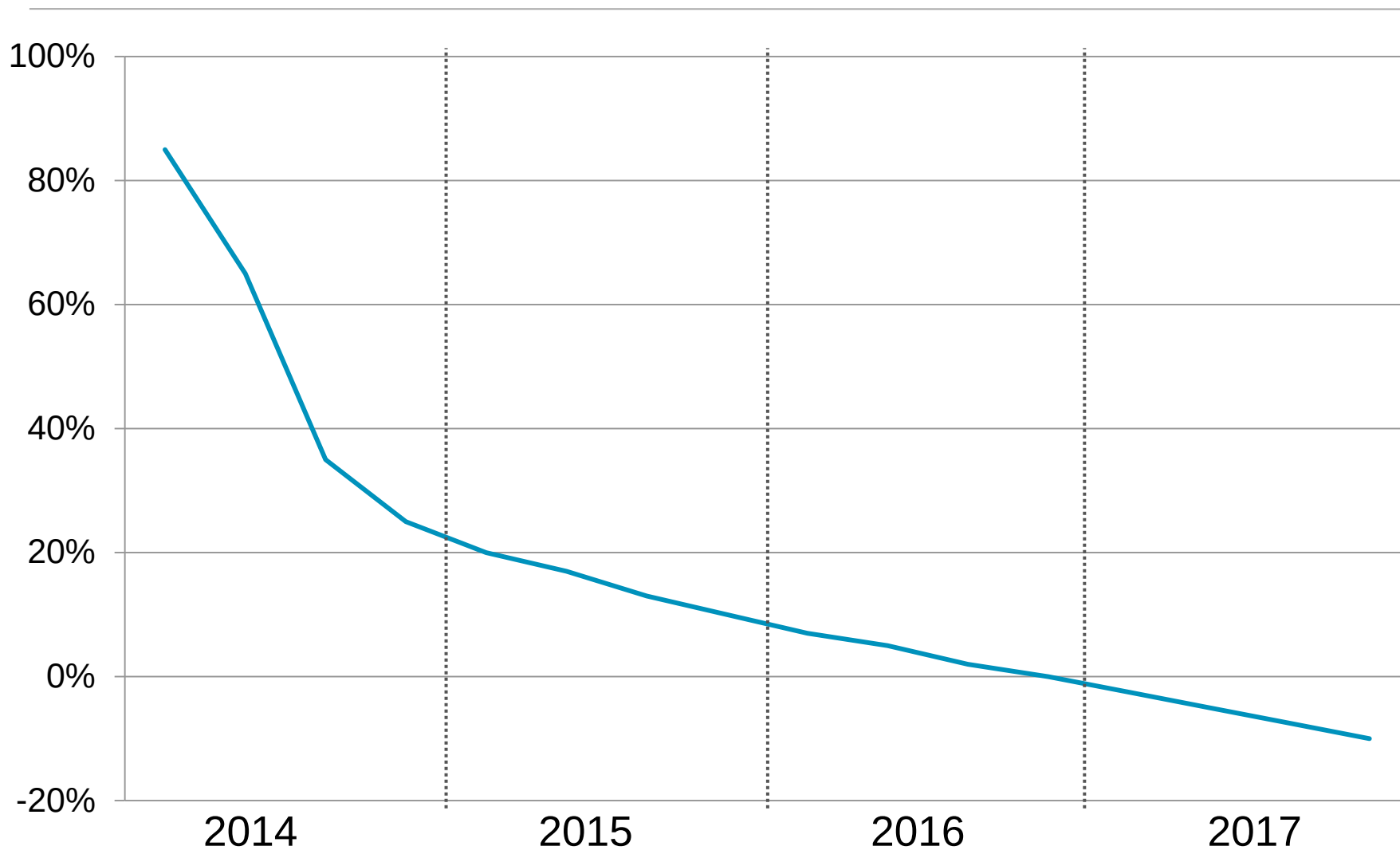
* Not supported in UltraScale

DDR3 vs. DDR4: Performance in UltraScale

Features	DDR3 /L	DDR4	DDR4 Improvements
Data rate (Mb/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, 2667 3200	13% 50% faster
Densities	512Mb to 8Gb	2Gb to 16Gb	2x density in a single chip
Internal Banks	8	16 (x4,x8) 8 (x16)	More banks (x4, x8)
Bank groups	0	4 (x4, x8) 2 (x16)	Faster burst accesses

* Not supported in UltraScale

DDR4 vs. DDR3: Price Premium



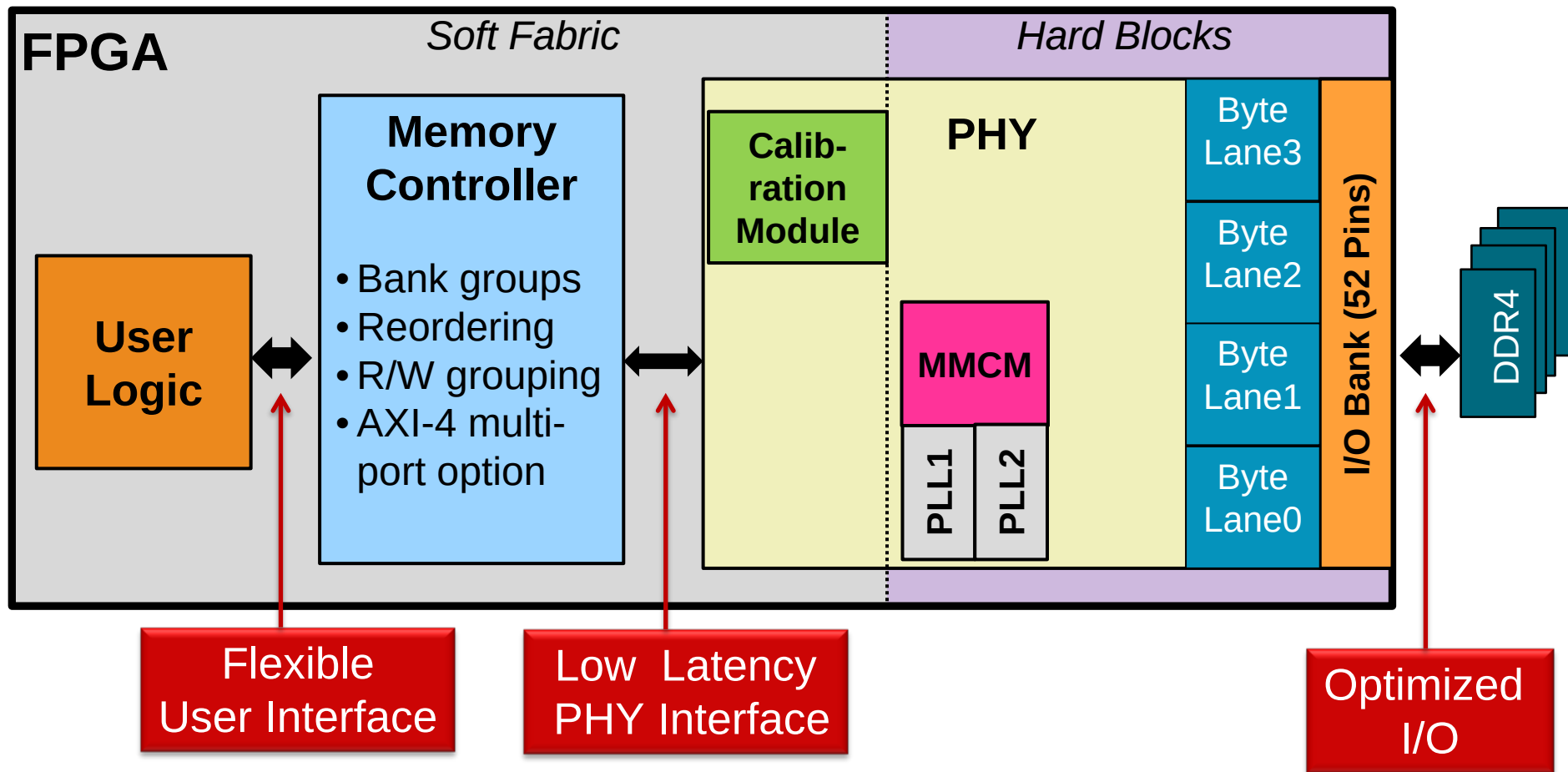
* Estimate courtesy Micron

UltraScale Memory Interface Features

UltraScale Memory Interface Support

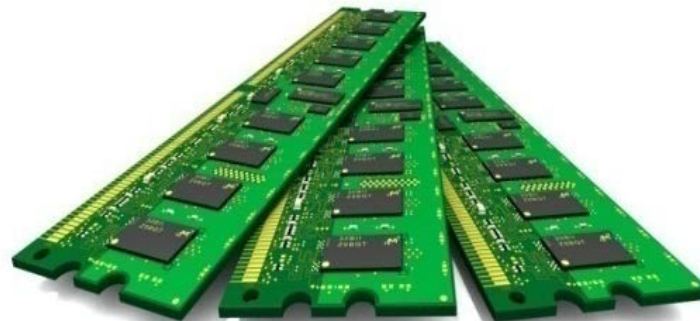
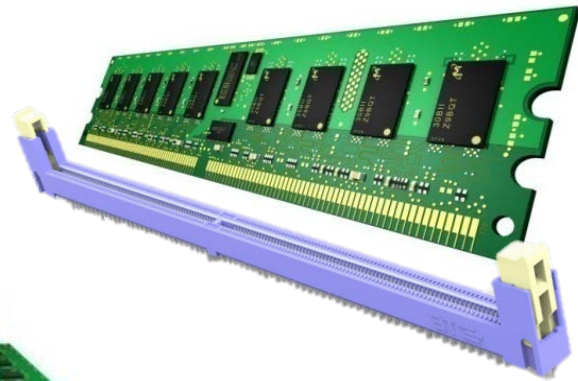
Memory	UltraScale Support
DDR4	1200 MHz
DDR3	1067 MHz
DDR3L	933 MHz
LPDDR3	TBD
QDR II+ (Xtreme)	633 MHz
QDR IV	TBD
RLDRAM 3	1066 MHz

UltraScale Memory Interface Architecture



UltraScale DDR4 DIMM Support

- x16, x8, and x4-based DIMMs
- Single, dual, and quad rank DIMMs
- DIMM types supported
 - SODIMM
 - UDIMM
 - RDIMM



Vivado® DDR4 DIMM Support

DDR4 DIMM Type	Vivado Support Schedule*
SODIMM (1R, 2R)	2014.3
UDIMM (1R, 2R)	2014.3
RDIMM (1R, 2R)	2015.1
RDIMM (4R)	2015.2

Notes:

- Release version for support is subject to change
- No current plans for an UltraScale development board with DDR4 DIMM

System Design-in Considerations for DDR4 with UltraScale

High-Speed PCB Design

- Understand transmission line theory
- Match trace lengths
- Control impedances
- Use proper termination
- Utilize best practice power supply design
 - Bypass properly
 - Avoid crossing splits in the power plane
- Reduce noise on V_{REF}
- Engineer the layout to minimize crosstalk

UltraScale Architecture PCB Design

Advance Specification User Guide

UG583 (v1.1) August 28, 2014

Read and
follow
UG583!

High-Speed PCB Design

- Understand transmission line theory
- Match trace lengths

UltraScale Architecture
PCB Design

“Strict adherence to all documented DDR4 PCB guidelines is required for successful operation.”

Engineer the layout to
minimize crosstalk

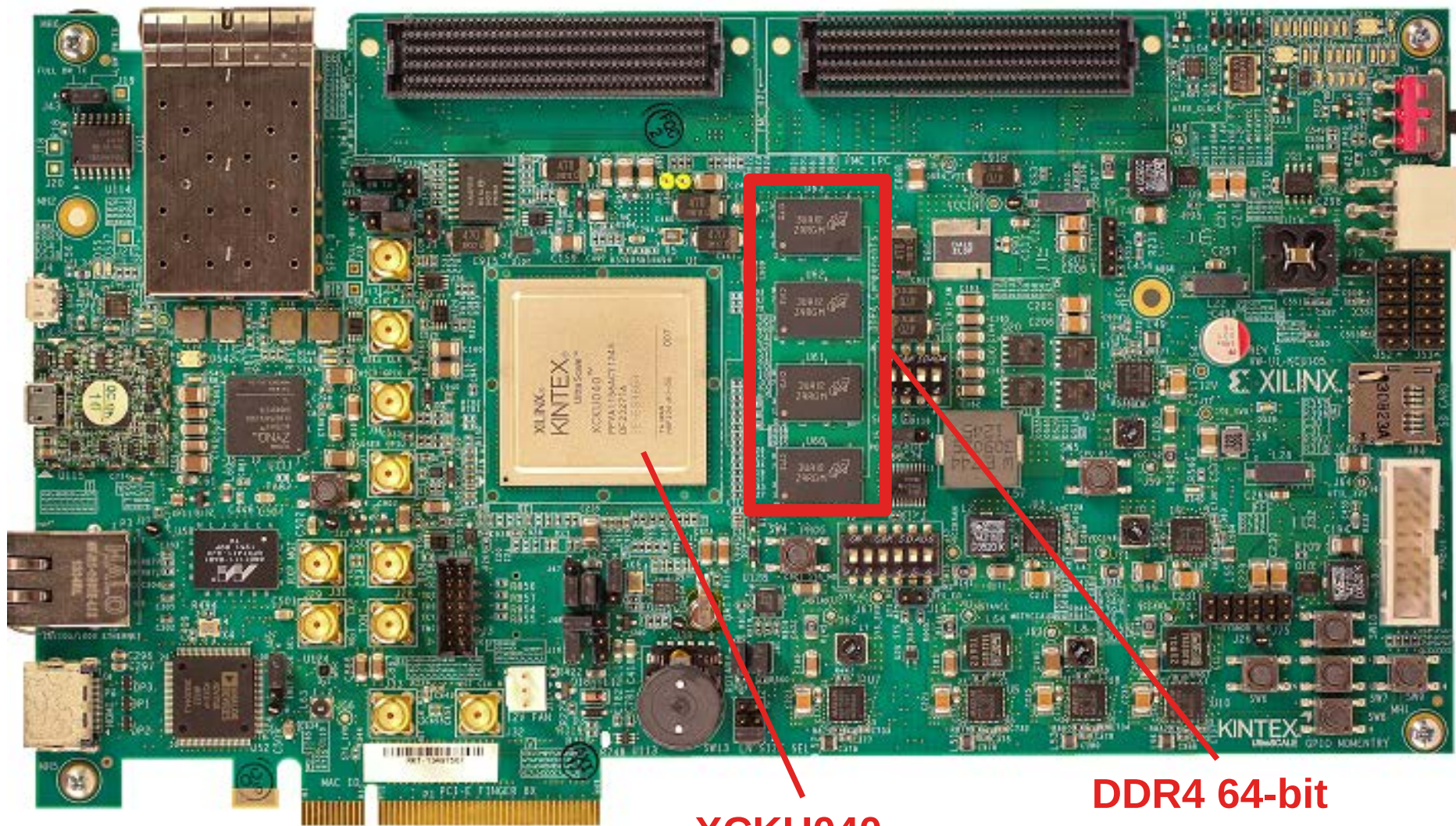
UG583!



DDR4 Design Checklist – XTP359

File		Home		xtp359-MIG-IP-UltraScale-Design-Checklist.xlsx - Microsoft Excel		
C8		ID	Description			
A		2.1	PCB Layout Requirements			
1		2.1.1	Reference Stack-Up			
2			Have you followed all signal routing layer and reference stack-up requirements?			
3		2.1.2	Topology and Routing Guidelines			
Instructions:			Are you following the required fly-by termination, impedance, length, and spacing guidelines for addr/cmd/ctrl?			
			Are you following the required fly-by termination, impedance, length, and spacing guidelines for clock signals?			
			Are you following the point to point required routing for data signals?			
			Are you following the required length routing constraints?			
			Are you following the required length matching routing constraints?			
			Package Delays must be included in length matching. Package delays can be found within the Vivado Pinout Table.			
			Are you following MIG routing guidelines?			

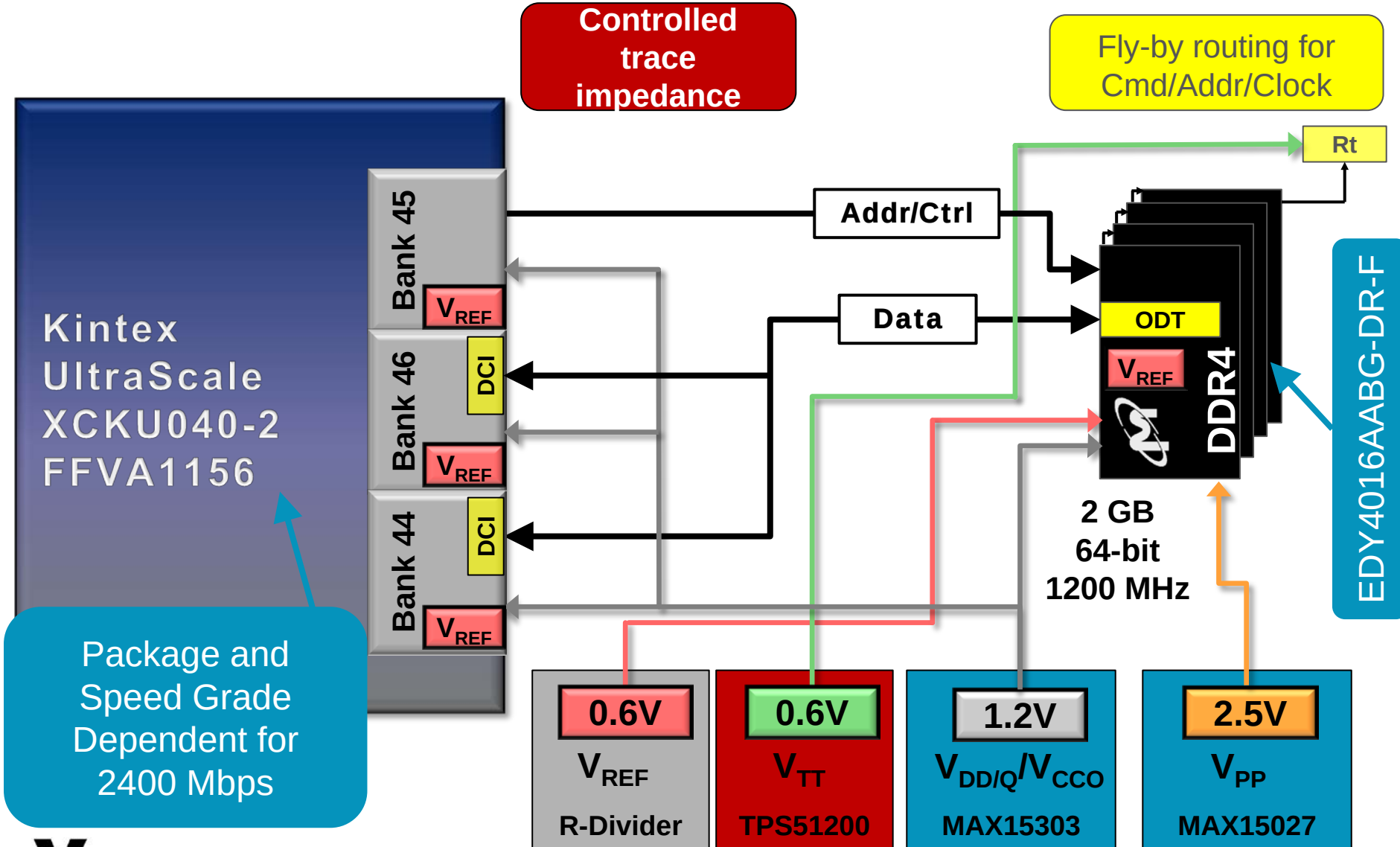
Design Example: KCU105 Board



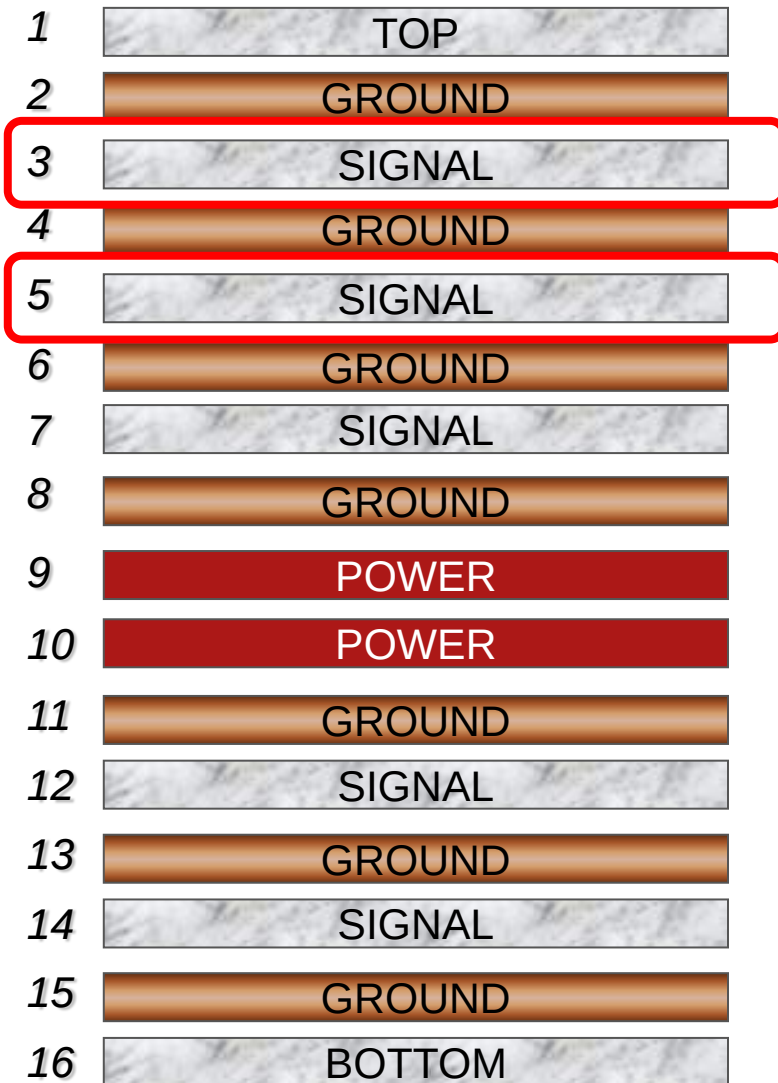
**XCKU040-
2FFVA1156**

**DDR4 64-bit
EDY4016AABG-DR-F**

KCU105 Memory Interface PCB Design



Stack-up Recommendation (KCU105)



To achieve highest memory interface performance

⑩ DDR4 signals must be routed on the top signal layers, that is, L3/L5

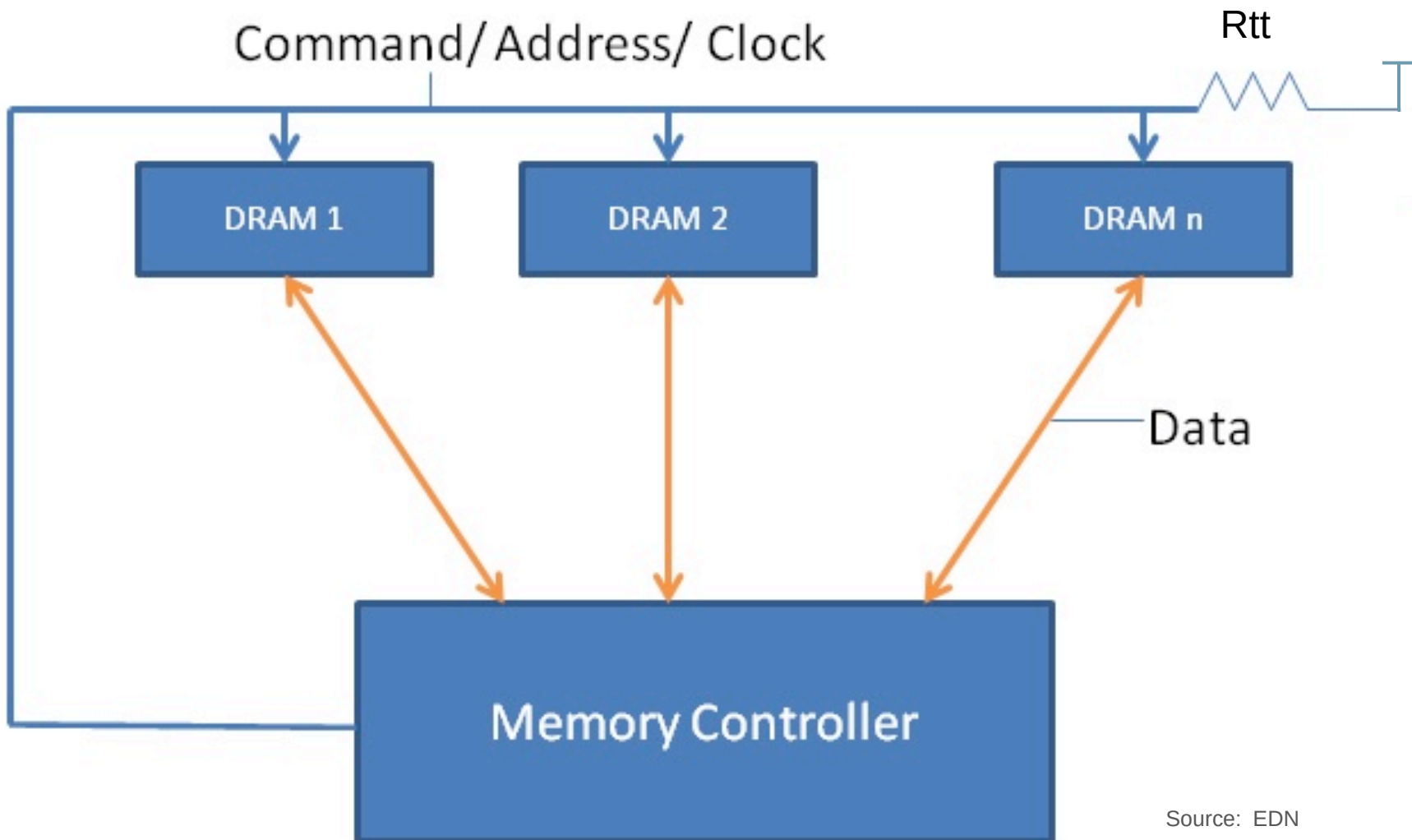
Notice

⑩ All DDR4 components and UltraScale should be on the top side

⑩ No adjacent signal layers

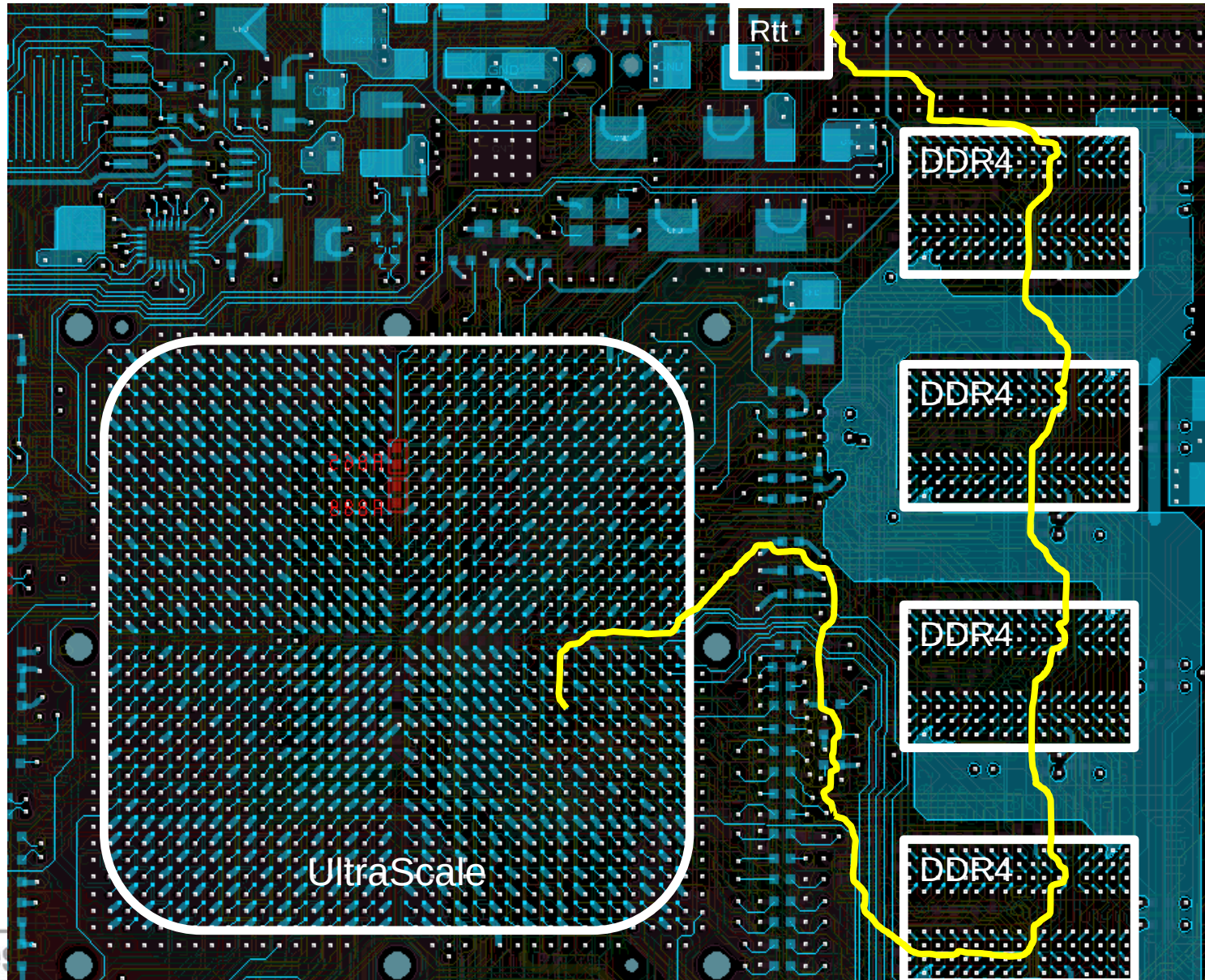
⑩ All reference planes are GROUND

Fly-By Routing



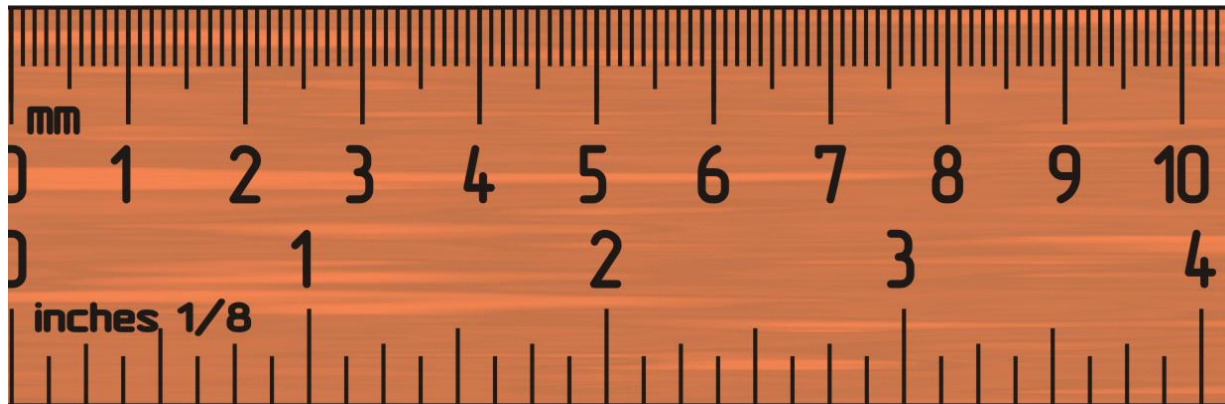
Source: EDN

KCU105 Fly-by



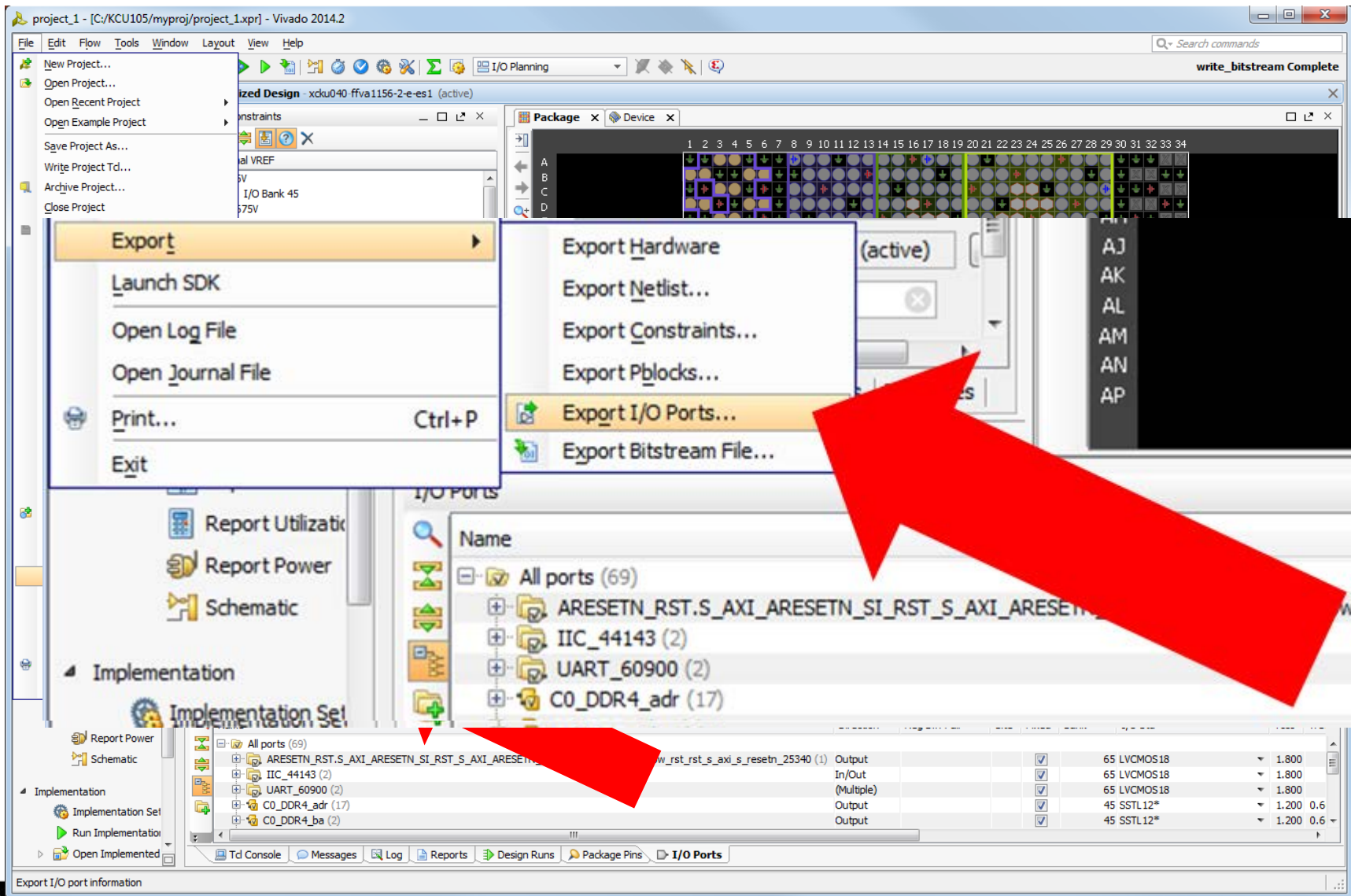
Trace Length Matching

- All DDR4 signals have min/max length requirements
- All DDR4 signals must be matched within groups
- Example: DQs within a data group
 - Match within +/- 15 mil
 - MUST include internal package delays
 - In Vivado, open synthesized design, then...





File → Export → Export I/O Ports



KCU105 Trace Length Matching Example

■ PCB flight time

- Microstrip $\rightarrow 136 \text{ ps/in} = 0.136 \text{ ps/mil}$
- Stripline $\rightarrow 170 \text{ ps/in} = 0.17 \text{ ps/mil}$

■ Specification: $\pm 15 \text{ mil} = \pm 2.55 \text{ ps}$

Signal	UltraScale Pin	Package Flight Time (ps)	KCU105 Flight Time (ps)			Total (ps)	Difference
			Top	L5	Top		
DQ0	AE23	70.274	3.944	422.957	3.029	500.20	1.79 ps 
DQ1	AG20	87.335	3.944	404.102	3.029	498.41	

Creating an UltraScale DDR4 Memory Controller

Generating the Xilinx MIG DDR4 Controller

■ Memory Interface Generator (MIG)

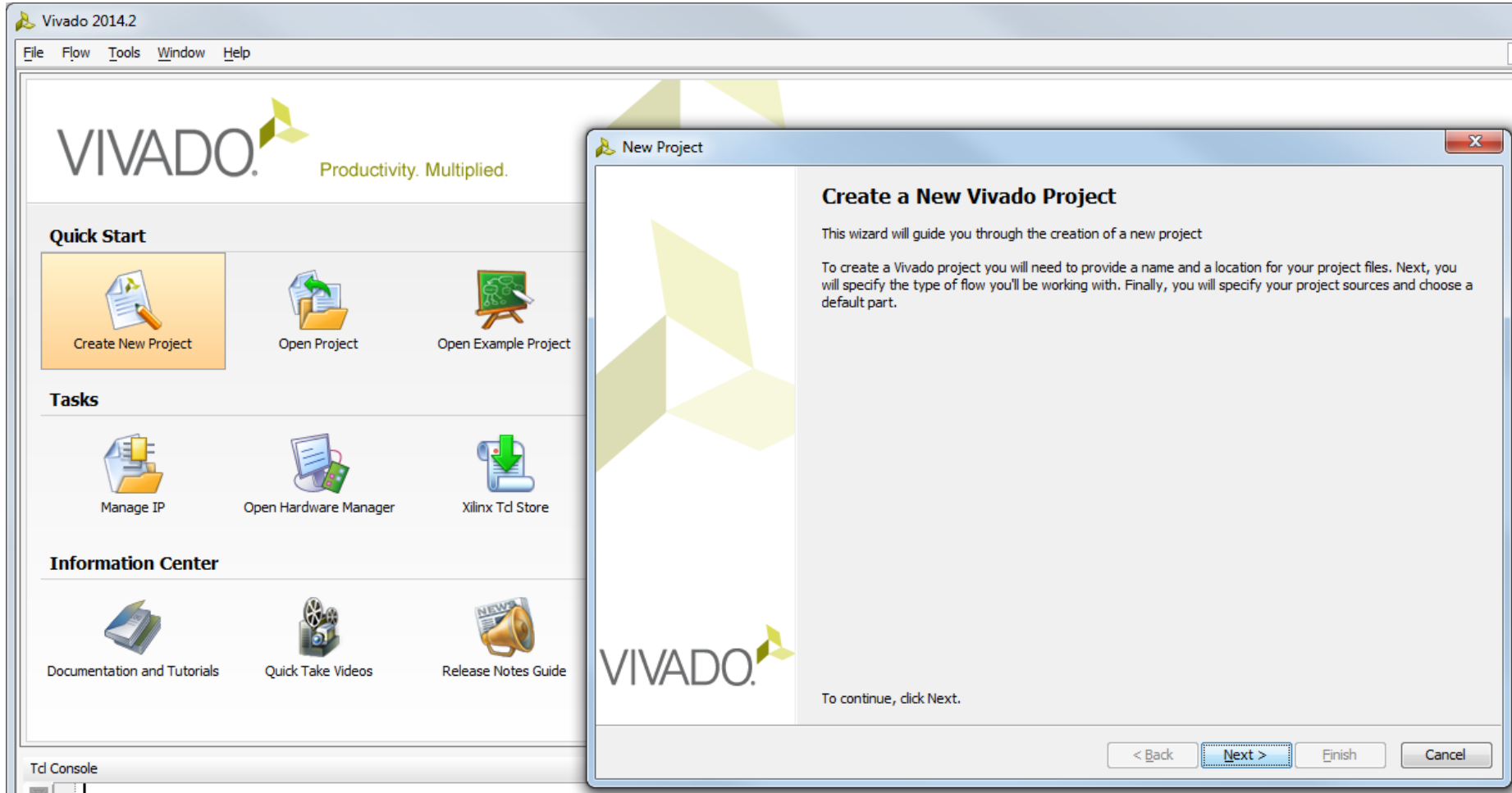
- Launched from Vivado IP Catalog
- Interface parameter selection
 - Device, burst length, data interleaving, re-ordering

■ Generated outputs

- HDL Code: Verilog (no VHDL)
 - User interface: AXI or User
- Simulation support
- Build parameters
- Example design
 - Simulate or synthesize



MIG Demo – Create New Project



MIG Demo – Select Kintex UltraScale Device

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Specify

Filter

Product category: All Package: ffva1156

Family: Kintex UltraScale Speed grade: -2

Sub-Family: All Remaining Temp grade: I

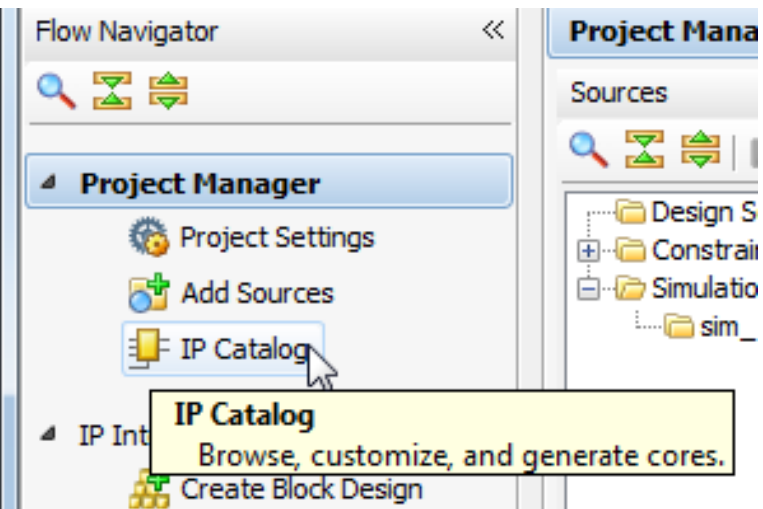
Reset All Filters

Search: Q

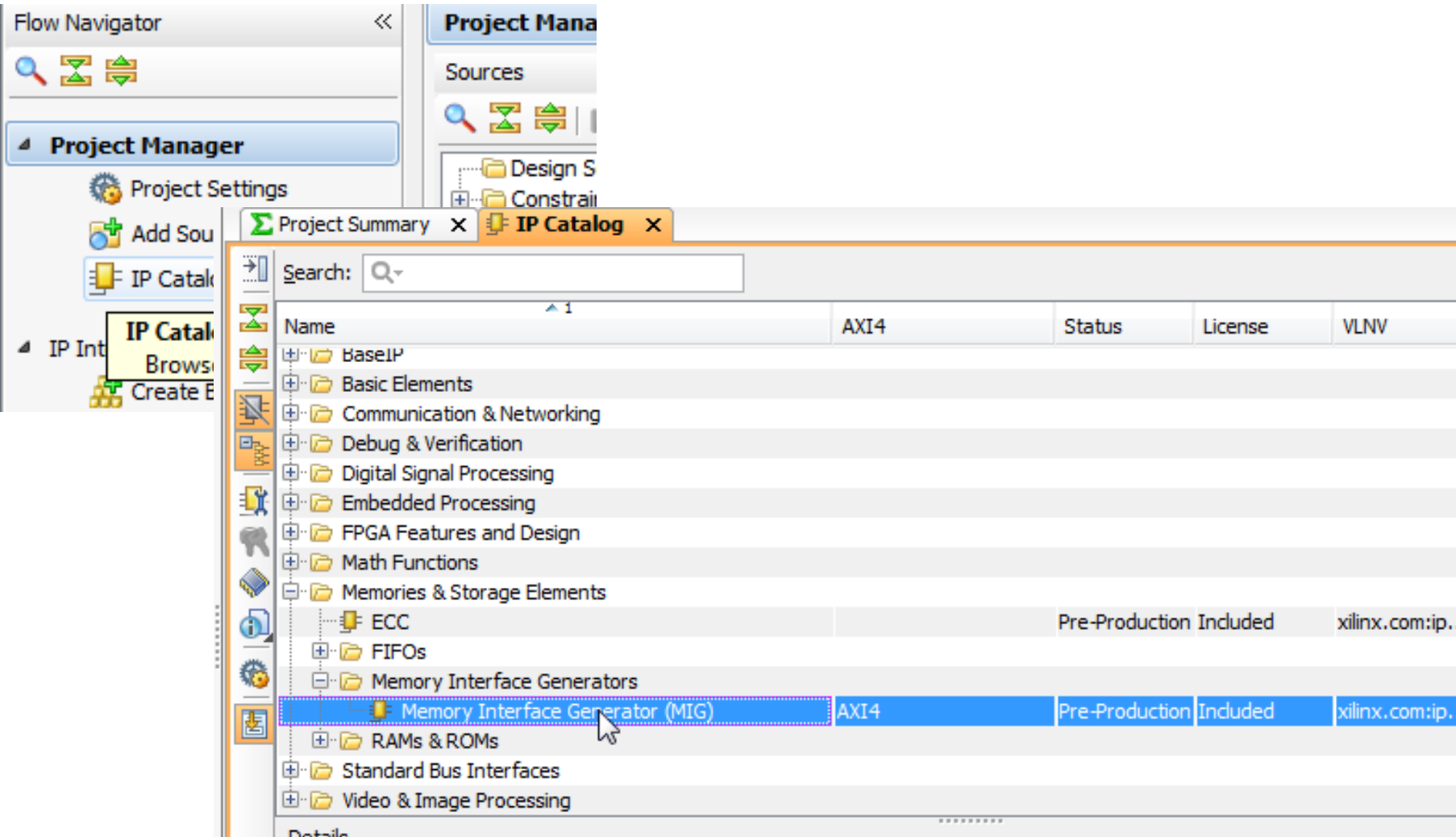
Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	DSPs	Gb Transceivers	GTHE Trans
xcku035-ffva1156-2-i-es1	1,156	520	203128	406256	540	1700	16	16
xcku040-ffva1156-2-i-es1	1,156	520	242400	484800	600	1920	20	20
xcku060-ffva1156-2-i-es1	1,156	520	331680	663360	1080	2760	28	28
xcku075-ffva1156-2-i-es1	1,156	520	432000	864000	1188	2592	28	28

< Back Next > Finish Cancel

MIG Demo – Launch IP Catalog, Select MIG



MIG Demo – Launch IP Catalog, Select MIG



The screenshot shows the Xilinx IDE interface. On the left is the 'Project Manager' pane. The main window displays the 'IP Catalog' tab. A search bar is at the top of the catalog. Below it is a list of IP categories and specific IP blocks. The 'Memory Interface Generator (MIG)' is highlighted. Below the list, the 'Details' section shows the name of the selected IP.

Name	AXI4	Status	License	VLNV
BaseIP				
Basic Elements				
Communication & Networking				
Debug & Verification				
Digital Signal Processing				
Embedded Processing				
FPGA Features and Design				
Math Functions				
Memories & Storage Elements				
ECC		Pre-Production	Included	xilinx.com:ip...
FIFOs				
Memory Interface Generators				
Memory Interface Generator (MIG)	AXI4	Pre-Production	Included	xilinx.com:ip...
RAMs & ROMs				
Standard Bus Interfaces				
Video & Image Processing				

Details

Name: **Memory Interface Generator (MIG)**

MIG Demo – Add DDR4 SDRAM Interface

Memory Interface Generator (MIG) (5.0)

Documentation IP Location Advanced Switch to Default

IP Symbol Resources

I/O planning status	NA
I/O ports count	NA
Assigned ports count	0
Package pins count	520
Banks available	NA

Component Name mig_0

Welcome to Memory Interface Generator Wizard (MIG)

Select Controller

Controller	Name	Family	Frequency(MHz)	DataWidth

Add

Delete

DDR4_SDRAM

DDR3_SDRAM

RLDRAM3

QDRIIPLUS_SDRAM

Click 'Add' to add a controller.

MIG Demo – Add DDR4 SDRAM Interface

Memory Interface Generator (MIG) (5.0)

Documentation IP Location Advanced Switch to Default

IP Symbol Resources

I/O planning status	NA
I/O ports count	NA
Assigned ports count	0
Package pins count	520
Banks available	NA

Component Name mig_0

Welcome to Memory Interface Generator Wizard (MIG)

Select Controller

Controller	Name	Family	Frequency(MHz)	DataWidth

Add

Delete

DDR4_SDRAM

DDR3_SDRAM

RLDRAM3

QDRIIPLUS_SDRAM

Click 'Add' to add a controller.

Component Name mig_0

Welcome to Memory Interface Generator Wizard (MIG)

Select Controller

Controller	Name	Family	Frequency(MHz)	DataWidth	Memory Part
C0	MainMemory	DDR4_SDRAM	1200.4801	8	MT40A256M16HA-083

Add

Delete

MIG Demo – Set Parameters

Component Name

C0.DDR4.Controller

Clocking

Clock Period (ps) ✕
 (833 ps = 1200 MHz) Range:[833..1600]

Input Clock Period (ps) ▼
 (3333 ps = 300 MHz)

Fabric to Memory Clock Ratio ▼

Controller Options

Configuration ▼

Memory Part ▼

IO Memory Voltage ▼

Data Width ▼

☒ Data Mask

Memory Address Map ▼

Memory Options

Burst length ▼

Cas Latency ▼

Cas Write Latency ▼

☒ Chip Select

Component Name

Common

FPGA Options

System Clock Configuration ▼

☒ Internal Vref

Debug Signals for controller

☐ Disable

☒ Enable

Clock Options

MIG can generate up to 4 additional clocks to be used in Fabric logic. This will be generated from the same MMCM which is used for generation of UI CLK. All the values in the additional clocks drop downs are calculated considering the selected MMCM VCO frequency in Mhz. For complete details on clocking of MIG, refer to MIG product Guide.

Clock 1 (MHz) ▼ D = 0

Clock 2 (MHz) ▼ D = 0

Clock 3 (MHz) ▼ D = 0

Clock 4 (MHz) ▼ D = 0

MIG Demo – Floorplan

Basic I/O Planning

Name	Mem Byte Group	Bank Type
I/O Bank 46 (2/4 Used)		
Byte Group T3	C0.Address/Ctrl-0	High Performance
Byte Group T2	Unassigned	High Performance
Byte Group T1	C0.DQ[56-63]	High Performance
Byte Group T0	C0.DQ[48-55]	High Performance
I/O Bank 45 (4/4 Used)		
Byte Group T3	C0.DQ[40-47]	High Performance
Byte Group T2	C0.DQ[32-39]	High Performance
Byte Group T1	C0.Address/Ctrl-1	High Performance
Byte Group T0	Unassigned	High Performance
I/O Bank 44 (4/4 Used)		
Byte Group T3	C0.DQ[24-31]	High Performance
Byte Group T2	C0.DQ[16-23]	High Performance
Byte Group T1	C0.DQ[8-15]	High Performance

Error Window

Error: Address bytes are spread in more than one bank (45,46). All the Address bytes must be selected in single bank.

MIG Demo – Floorplan

Basic I/O Planning

Name	Mem Byte Group	Bank Type
I/O Bank 46 (2/4 Used)		
Byte Group T3	C0.Address/Ctrl-0	High Performance
Byte Group T2		
Byte Group T1		
Byte Group T0		
I/O Bank 45 (4/4 Used)		
Byte Group T3		
Byte Group T2		
Byte Group T1		
Byte Group T0		
I/O Bank 44 (4/4 Used)		
Byte Group T3		
Byte Group T2		
Byte Group T1		

Error Window

Error: Address bytes are spread in more tha

Bank Planning

Basic I/O Planning

Name	Mem Byte Group	Bank Type
I/O Bank 46 (4/4 Used)		
Byte Group T3	C0.DQ[56-63]	High Performance
Byte Group T2	C0.DQ[48-55]	High Performance
Byte Group T1	C0.DQ[40-47]	High Performance
Byte Group T0	C0.DQ[32-39]	High Performance
I/O Bank 45 (3/4 Used)		
Byte Group T3	Unassigned	High Performance
Byte Group T2	C0.Address/Ctrl-2	High Performance
Byte Group T1	C0.Address/Ctrl-1	High Performance
Byte Group T0	C0.Address/Ctrl-0	High Performance
I/O Bank 44 (4/4 Used)		
Byte Group T3	C0.DQ[24-31]	High Performance
Byte Group T2	C0.DQ[16-23]	High Performance
Byte Group T1	C0.DQ[8-15]	High Performance

MIG Demo – Run MIG I/O Pin Planner

Memory Interface Generator - I/O Pin Planning

Undo Redo Report DRC Unselect All

I/O Port Properties

Name: c0_ddr4_dq[63]
 Direction: In/Out
 Partition Pin: True
 Site: AM34 ☒ Fixed
 Site type: IO_L24N_T3U_N11_46
 Package pin: AM34
 Cell: c0_ddr4
 Net: c0_ddr4_dq[63]
 I/O Bank: I/O Bank 46
 Tile: HP10_L_X0Y150
 Clock region: X0Y2

I/O Ports

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref
c0_ddr4_cke (1)	Output			☒	45	SSTL12*	1.200	0.600
c0_ddr4_cs_n (1)	Output			☒	45	SSTL12*	1.200	0.600
c0_ddr4_dm_dbi_n (8)	In/Out			☒	(Multiple)	POD12_DCI*	1.200	0.840
c0_ddr4_dq (64)	In/Out			☒	(Multiple)	POD12_DCI*	1.200	0.840
c0_ddr4_dq[63]	In/Out		AM34	☒	46	POD12_DCI*	1.200	0.840
c0_ddr4_dq[62]	In/Out		AK1	☒	46	POD12_DCI*	1.200	0.840
c0_ddr4_dq[61]	In/Out		AK2	☒	46	POD12_DCI*	1.200	0.840
c0_ddr4_dq[60]	In/Out		AK5	☒	46	POD12_DCI*	1.200	0.840
c0_ddr4_dq[59]	In/Out		AK6	☒	46	POD12_DCI*	1.200	0.840

Port: c0_ddr4_dq[63]
 Direction: In/Out (partition pin)
 Net: c0_ddr4_dq[63]
 BEL: PAD
 Site: AM34 (fixed)
 Site type: IO_L24N_T3U_N11_46
 Tile: HP10_L_X0Y150
 Package pin: AM34
 I/O Bank: I/O Bank 46

Apply Constraints Discard Changes

MIG Demo – Summary

MIG Configuration Summary

FPGA Options

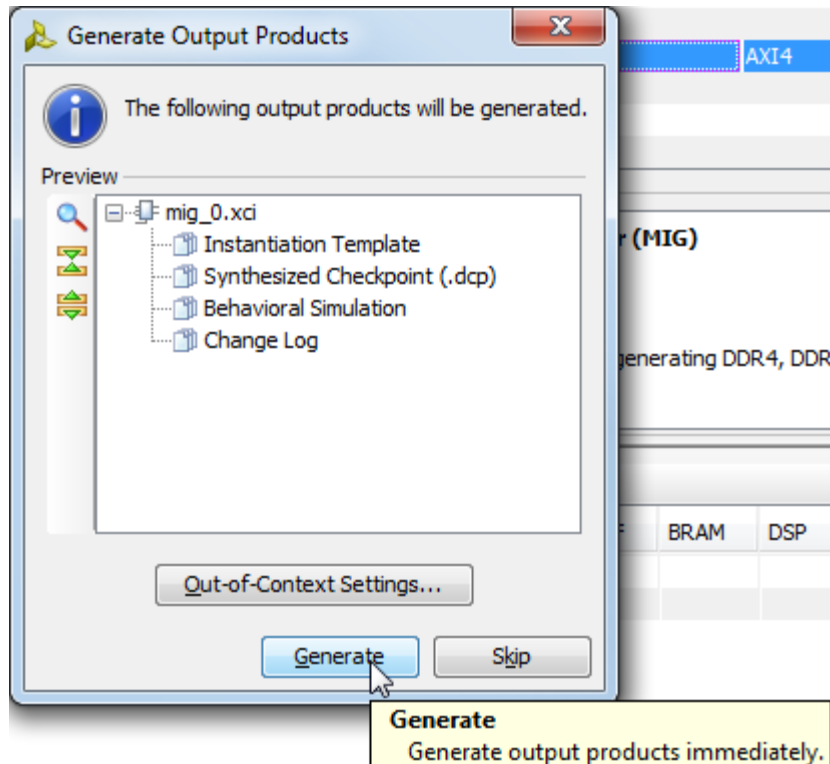
System Clock Type:	Differential
Reference Clock Type:	Differential
Internal Vref:	true

Controller Options

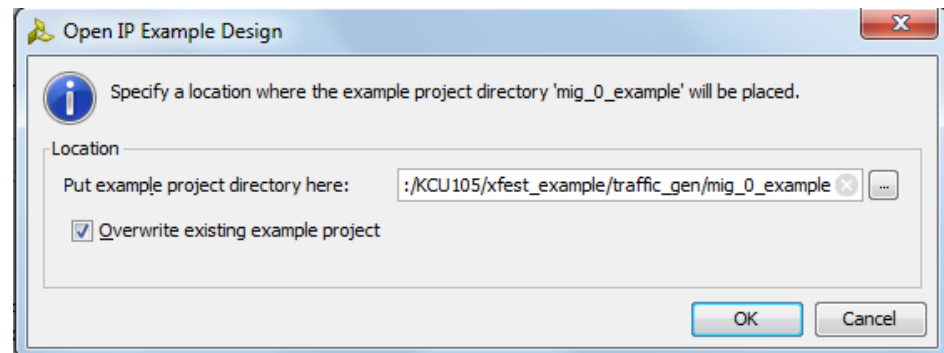
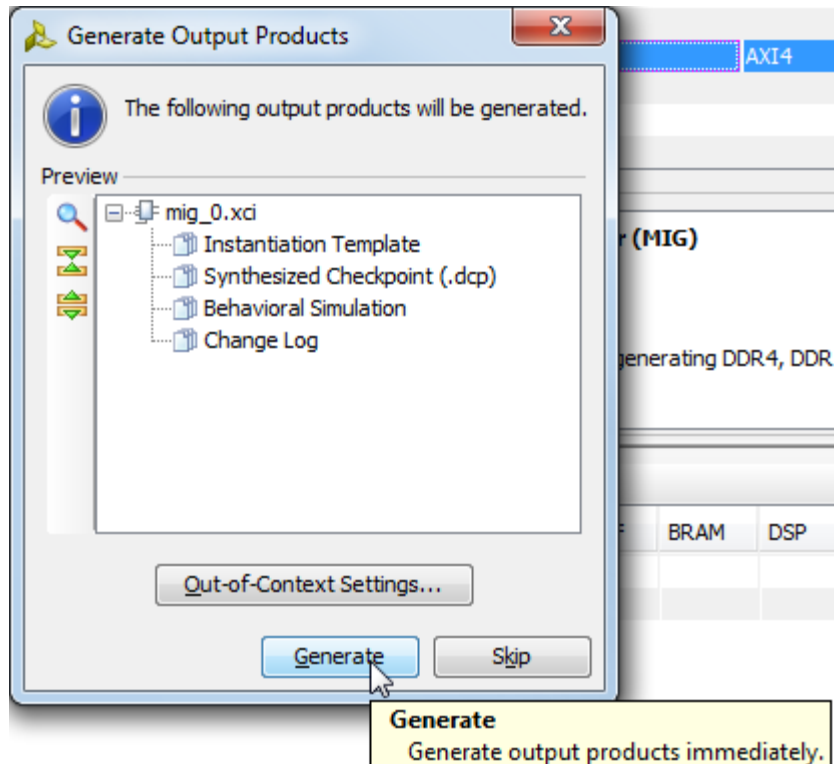
Controller 0

Memory:	DDR4_SDRAM
Design Clock Frequency:	(833 ps = 1200 MHz)
Phy Controller to Clock Ratio:	4:1
Input Clock Period:	(3333 ps = 300 MHz)
Memory Type:	Components
Memory Part:	MT40A256M16HA-083
Data Width:	64
Data Mask:	Enabled
Memory Address Map	BANK ROW COLUMN
Debug Signal for Memory Controller:	Enabled

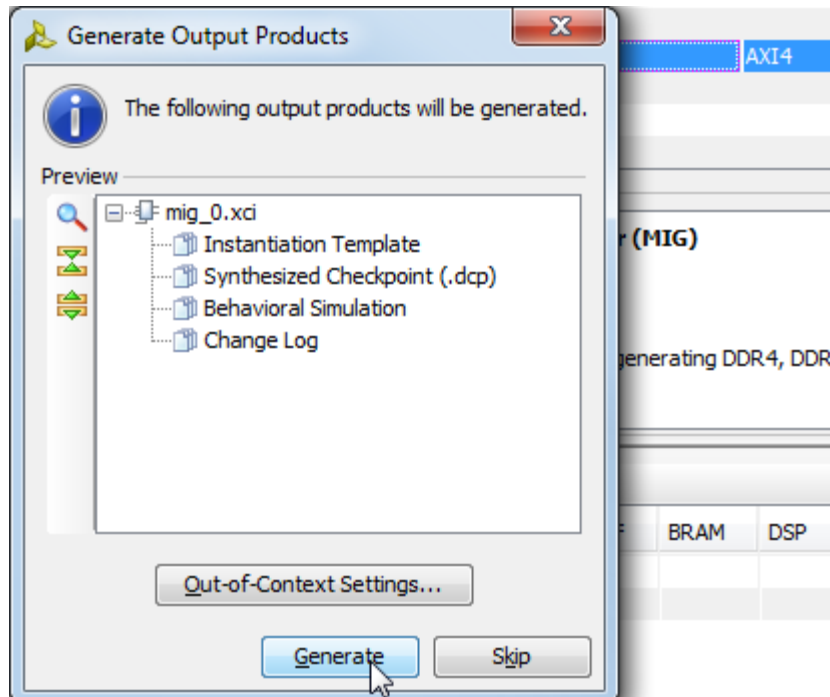
MIG Demo – Generate Controller and Example



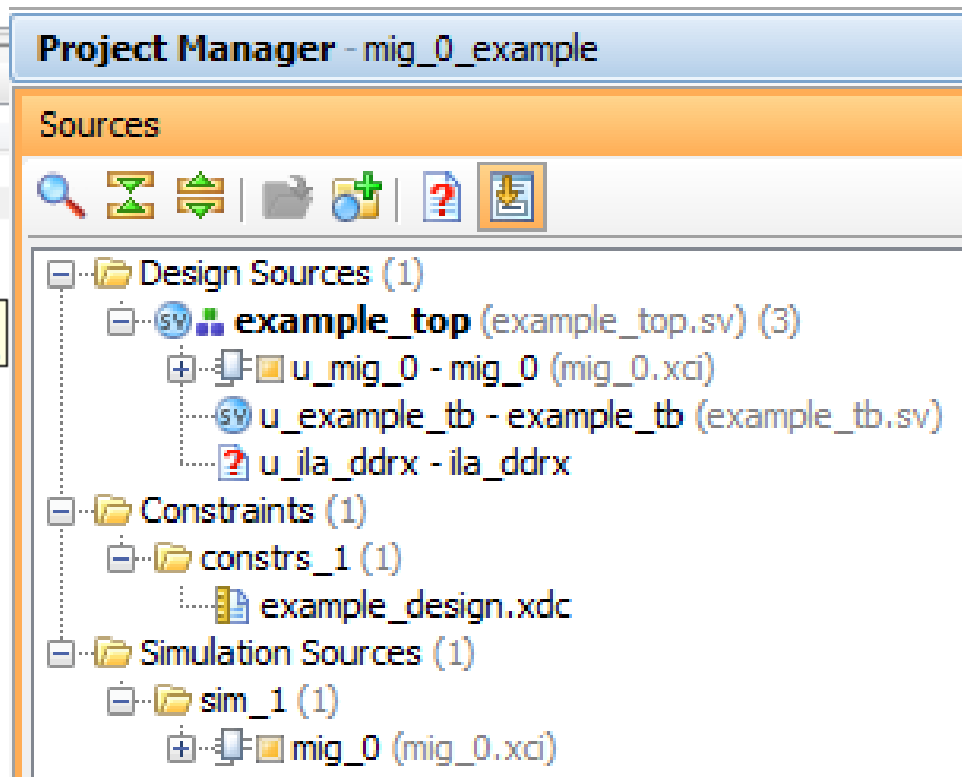
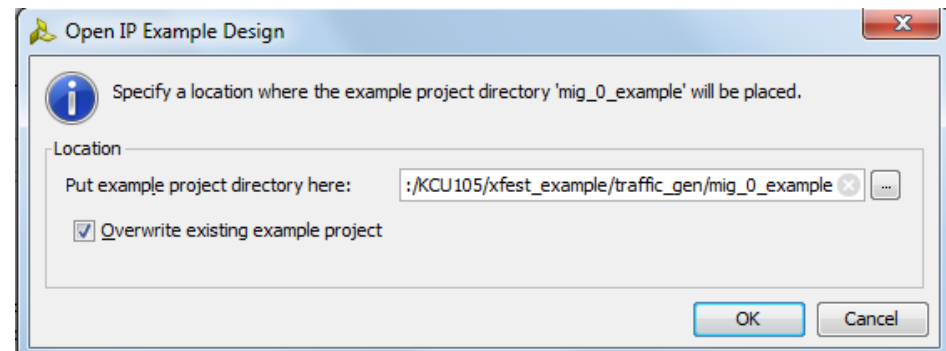
MIG Demo – Generate Controller and Example



MIG Demo – Generate Controller and Example



Generate
Generate output products immediately.



MIG Demo Summary

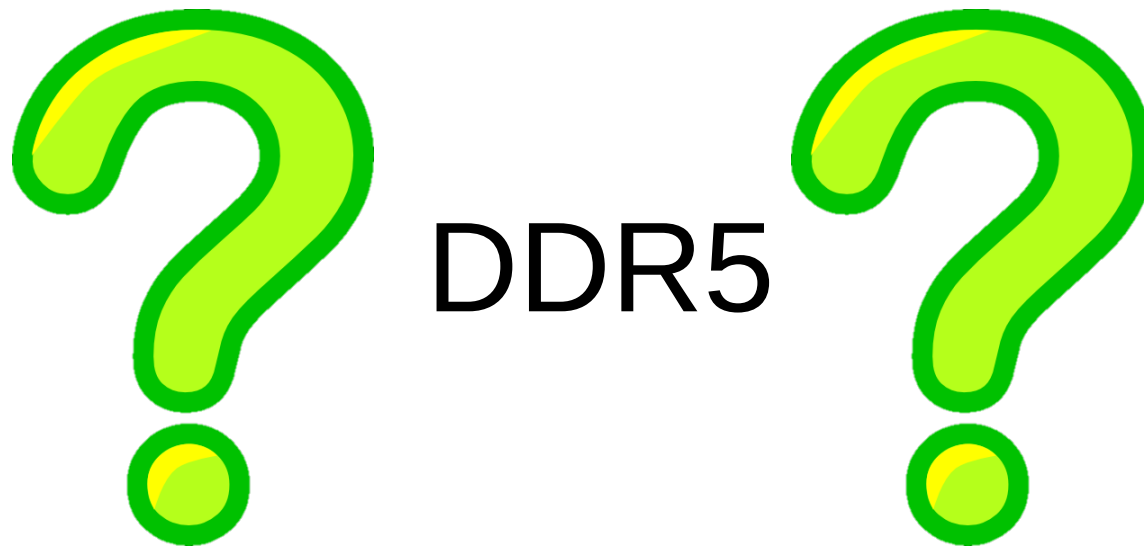
- **Build custom memory interfaces with MIG**
- **Generate the memory interface and controller quickly and easily**
- **Accelerate design productivity with MIG and the hardware-verified IP library**



Next Generation Memory

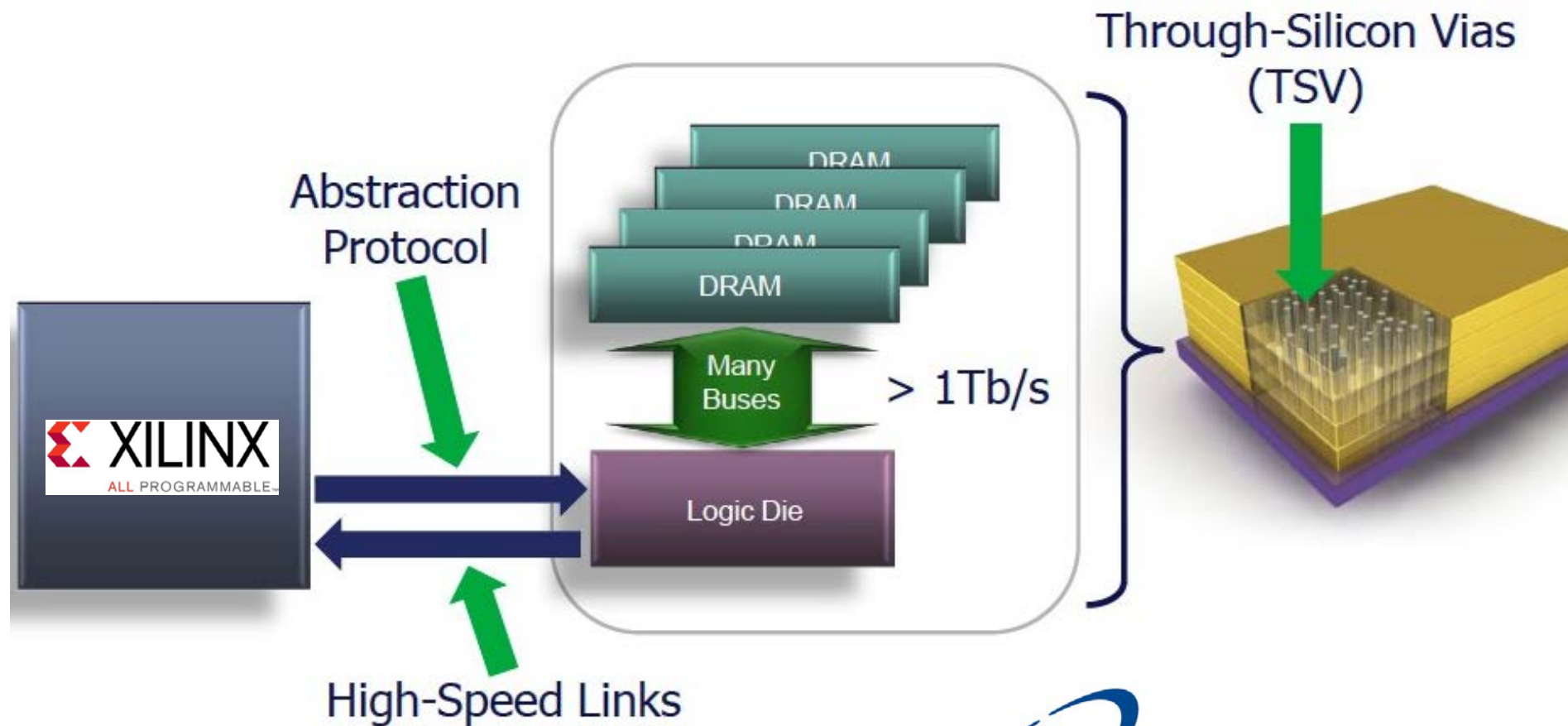


What comes after DDR4?



Hybrid Memory Cube

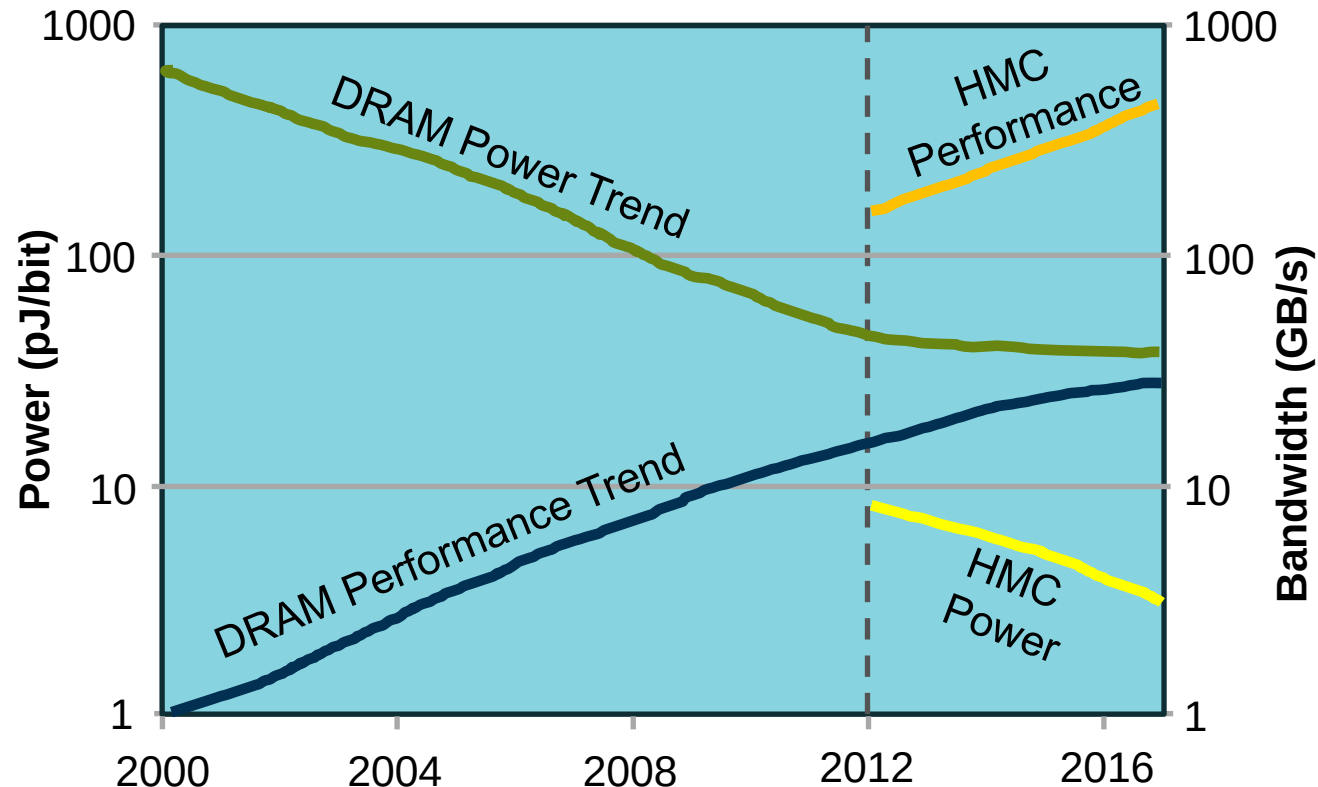
Hybrid Memory Cube (HMC)



Micron®

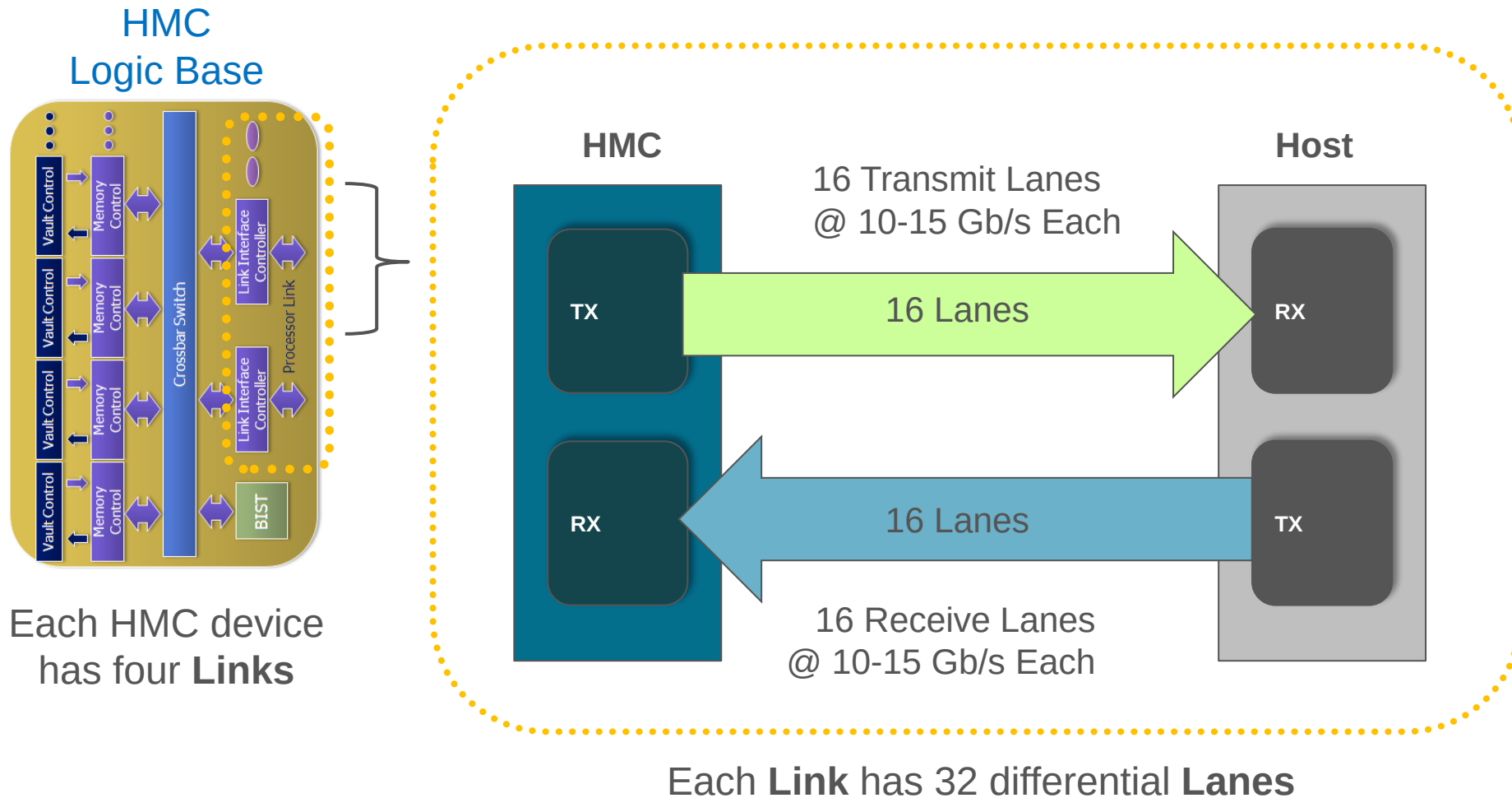
HMC Advantages over DRAM

- **Reduced power**
 - Up to 70% less energy per bit
- **Fewer pins**
 - Up to 85% less pins
- **Reduced footprint**
 - 90% less space than today's RDIMM
- **Increased Bandwidth**
 - 15x the performance



*Compared to DDR3-1333

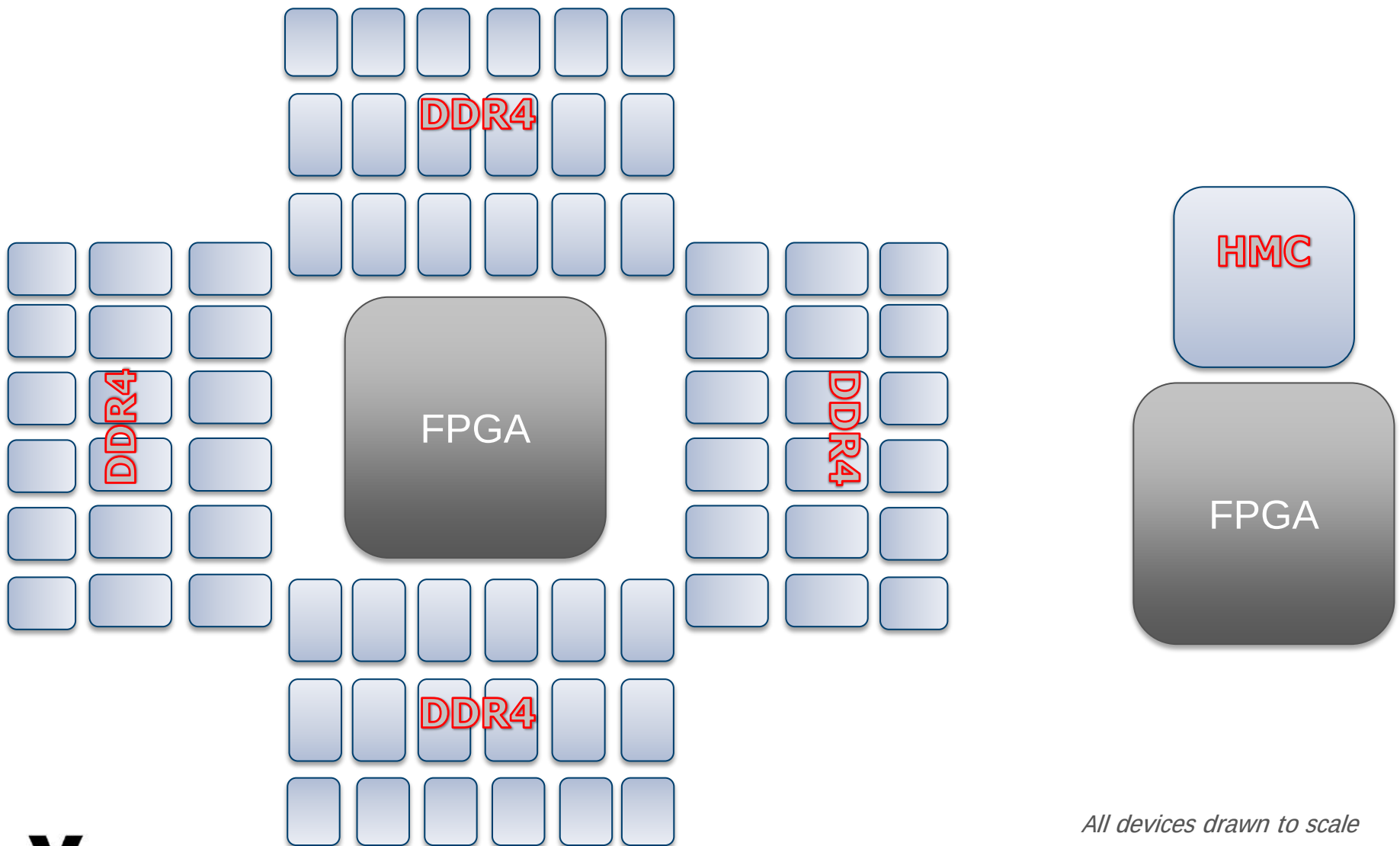
Link Controller Interface



400 Gbps Packet Buffer Example (with ECC)

Parameter	DDR4-2400	HMC 12.5G 4 Links	HMC Advantage
Number of Memory Devices	48 – x16 24 – x4	1	72 to 1
Total Number of Pins	1,896	276	85% fewer pins
Host PHY + Memory Power	49 W	32 W	35% lower power
Memory Surface Area	8,532 mm ²	961 mm ²	89% smaller footprint
Host PHY Silicon Area	1.75x	1x	75% smaller host PHY

400 Gbps Packet Buffer Comparison



All devices drawn to scale

IP Requirements

- **Virtex-7, Kintex UltraScale, or Virtex UltraScale**
- **10, 12.5, or 15 Gbps SERDES**
 - 16 SERDES for full Link (16 Tx / 16 Rx)
- **IP licensing**
 - Includes first year of maintenance and support
 - License fee per project



- Working example with Virtex-7
- Full-width Link (32 lanes) takes ~50K LUTs
- IP@Open-Silicon.com



- Working example with Kintex UltraScale – Pico EX-850 Board
- Full-width Link (32 lanes) takes ~35K LUTs
- Contact@picocomputing.com
- Other pricing upon request

Configuration	Price
Half-width 10G	\$40,000
Half-width 12.5G	\$45,000
Half-width 15G	\$50,000
Full-width 10G	\$50,000
Full-width 12.5G	\$60,000
Full-width 15G	\$70,000

Configuration	Price
Full-width 10G	\$65,000

Next Steps



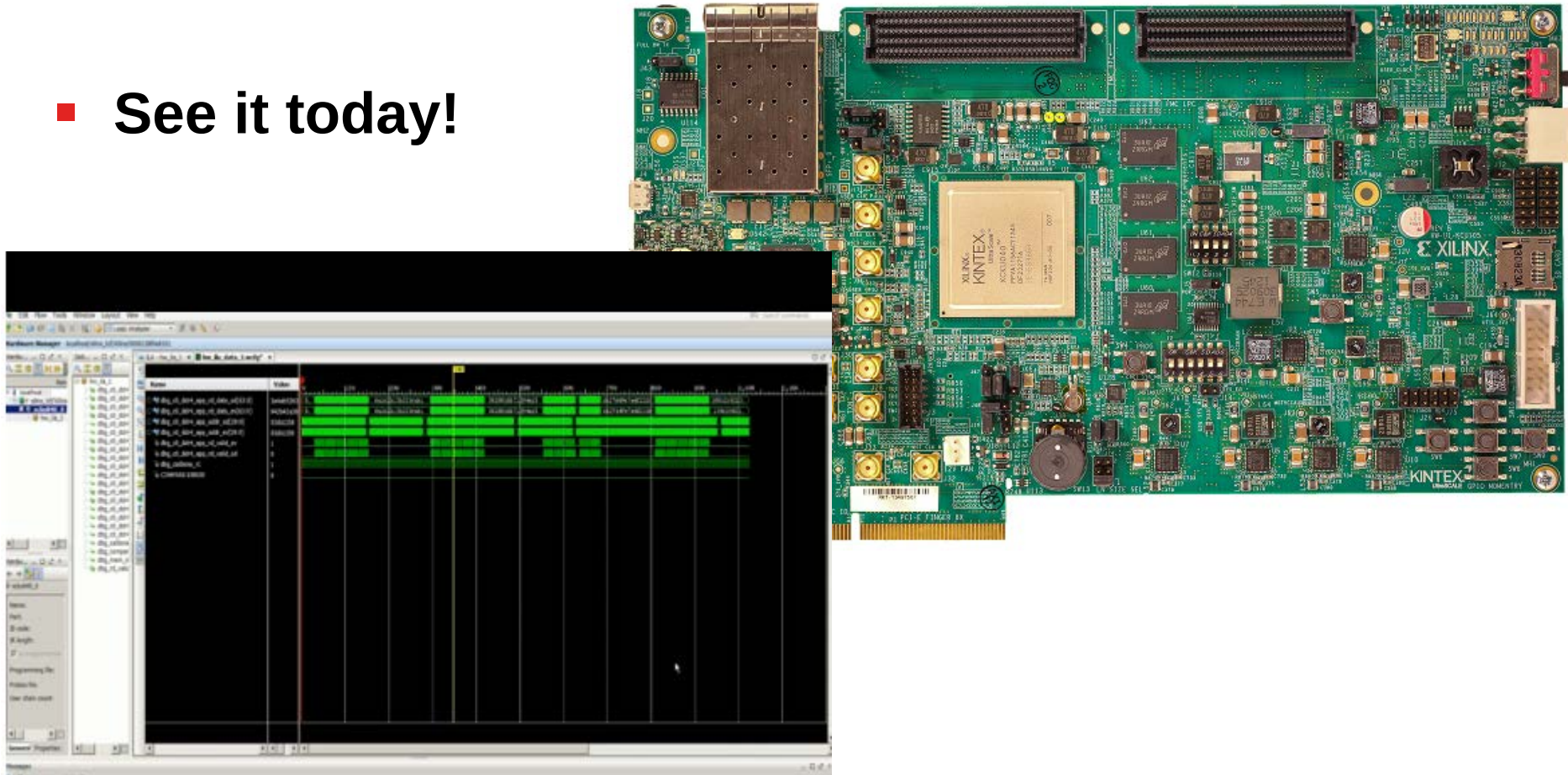
What Have We Learned?

- Major differences between DDR4 and DDR3
- Memories supported with UltraScale
- How to design an UltraScale DDR4 memory controller using MIG
- Preview next generation memory interfaces

How can you learn more?

See UltraScale and DDR4 Running at 2400 Mbps!

- KCU105 / DDR4-2400 demo on the Xilinx table
- See it today!



Buy the KCU105 Evaluation Kit

www.xilinx.com/KCU105

Cables and Power

Reference Designs and Docs



Kintex UltraScale KCU105
Evaluation Board

Vivado® Design Suite Development Tools

Ordering Information

Part Number:	EK-U1-KCU105-G
Price:	TBA
Shipping:	Q1 2015

Xilinx Two-day Course: *How to Design a High-Speed Memory Interface*

Accelerated Design
Productivity

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Or search the web for “**Xilinx Memory Interface Course**”

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www.xfest2014.com

- PDFs of all presentations
- Course forums

Reference Information on UltraScale DDR4

- <http://www.micron.com/products/dram/ddr4-sdram>
- <http://www.micron.com/products/support/power-calc>
- <http://www.micron.com/products/dram/ddr3-to-ddr4>
- www.xilinx.com/ultrascale
- http://www.xilinx.com/products/design_tools/logic_design/xpe.htm
- www.xilinx.com/kcu105
- **WP454 High-Performance, Lower-Power Memory Interfaces with UltraScale Architecture FPGAs**
- **PG150 LogiCORE IP UltraScale Architecture-Based FPGAs Memory Interface Solutions**
- **UG583 UltraScale Architecture PCB Design and Pin Planning**
- **UG917 KCU105 Board User Guide**
- <http://www.xilinx.com/products/technology/memory-interfacing/index.htm#uniquePlayer1>
- <http://www.xilinx.com/products/technology/memory-interfacing/index.htm#uniquePlayer2>
- <http://www.xilinx.com/training/ultrascale/designing-a-memory-interface-and-controller-with-vivado-mig-for-ultrascale.htm>
- www.xilinx.com/training/connectivity/designing-high-speed-memory-interfaces.htm
- <http://www.xilinx.com/support/answers/59625.html>

Reference Information on UltraScale HMC

- <http://www.micron.com/products/hybrid-memory-cube>
- **Xcell Journal, Issue 88 *Goodbye DDR, Hello Serial Memory***
- <http://picocomputing.com/products/hybrid-memory-cube-hmc-controller-ip/>
- <http://forums.xilinx.com/t5/Xcell-Daily-Blog/HMC-demo-shows-15Gbps-operation-per-link-at-last-month-s/ba-p/488174>
- <http://forums.xilinx.com/t5/Xcell-Daily-Blog/Hybrid-Memory-Cube-HMC-controller-and-interface-IP-rips-along-at/ba-p/480012>
- http://www.hotchips.org/wp-content/uploads/hc_archives/hc23/HC23.18.3-memory-FPGA/HC23.18.320-HybridCube-Pawlowski-Micron.pdf

Vinaka Maake Asante Shukria Dhanyavadagalu
 감사합니다 Dank Je Dankscheen Kam Sah Hammida Manana Dankon
 Blagodaram Ngiyabonga Dziekuje Mauruuru Biyan
 Juspaxar Chokrane Diolch i Chi Terima Kasih Matondo
 நன்றி Bedankt Dakujem Grazas cảm ơn bạn Tack
 Ua Tsaug Rau Koi Nirringrazzjak Hvala Di Ou Mesi Arigato Mochchakkeram
 Suksama Dėkuji Welalin Danke Kia Ora Paldies Tingki Gratias Tibi
 Misaotra Rahmat Matur Nuwun 谢谢 Obbrigado
 谢谢 Xbala Merci Go Raibh Maith Agat Eskerrik Asko
 Naiis Tuke

Thank You