
Chris Ammann

# Power and Thermal Design

Design considerations for your Xilinx FPGA / AP SoC



Accelerating Your Success™

# Capability is limited by the quality of your POWER

# Course Objectives

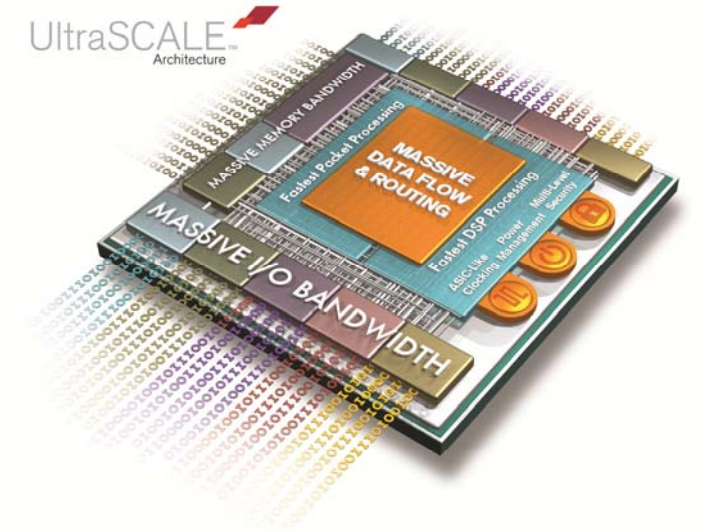
- Understand the requirements for designing the power architecture of Xilinx FPGA's / AP SoC's
- See how the design tools and resources available can aid in the development of a viable power solution for FPGA's / AP SoC's
- Understand the need for thermal relief, thermal affects on system performance and how to mitigate them
- Learn what reference material is available and where to find it

# Agenda

- FPGA and SoC power requirements
  - XPE demo
- Power system design
  - Regulation error
  - Transient response and decoupling
  - Transceiver power
  - Topologies
- Thermal impact on power design
  - Effects on components
  - Understanding heat sinking / thermal dissipation
- Design resources, examples and tools

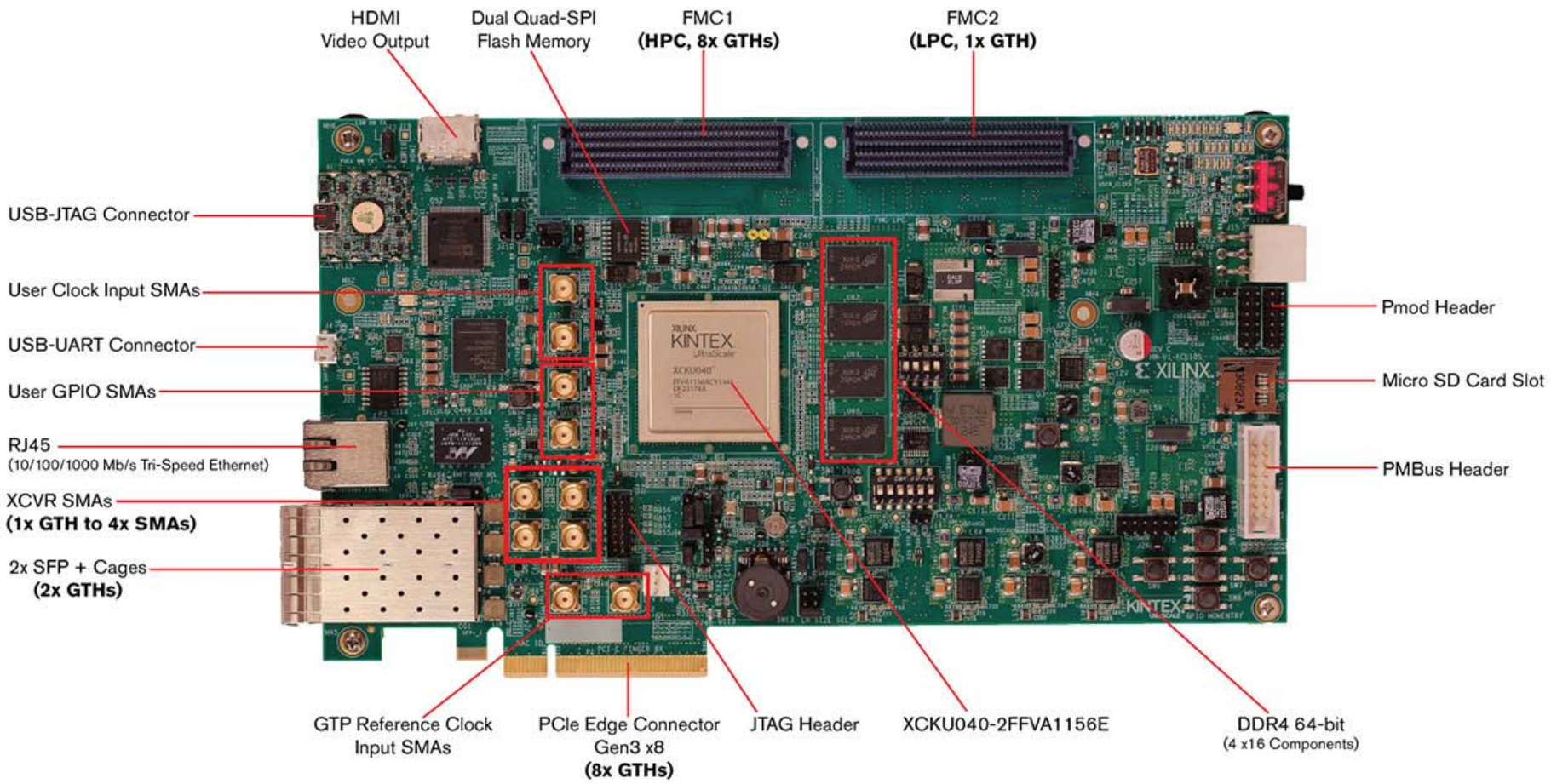
# UltraScale Power Saving Features

- Move from 28nm to 20nm technology
  - Lower core voltage (0.9V or 0.95V) and voltage scaling
  - Clock management
  - Power management of unused logic
  - Block RAM power savings
  - I/O and memory interface power reduction
  - Transceivers
    - Low power modes
- Refer to Xilinx WP451 for a full overview of power saving enhancements

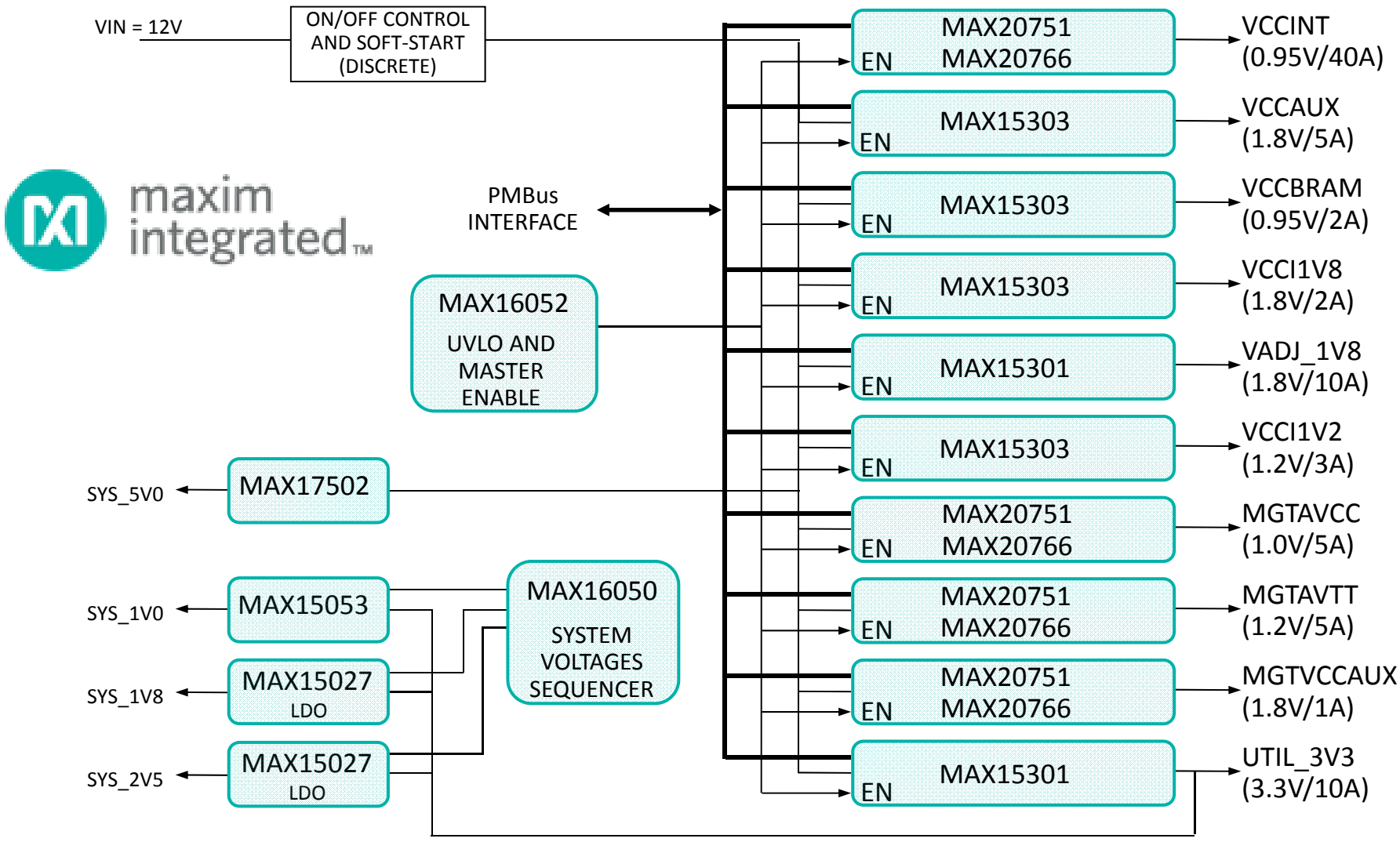


# UltraScale Kintex Development Board

- KCU105



# KCU105 Power Solution



# Voltage Requirements

| | ARTIX 7 | KINTEX 7 | VIRTEX 7 | ZYNQ | | UltraSCALE |
|---|---|---|---|---|---|---|
| Bank Name | All Devices | All Devices | All Devices | 7010/15 /20 | 7030/45 /100 | Kintex and Virtex Devices |
| $V_{CCINT}$ | 1V 5% | 1V 3% | 1V 3% | 1V 5% | 1V 3% | 0.9V 3% 0.95V 3% |
| $V_{CCINT\_IO}$ | | | | | | 0.9V 3% 0.95V 3% |
| $V_{CCBRAM}$ | 1V 5% | 1V 3% | 1V 3% | 1V 5% | 1V 3% | 0.95V 3% |
| $V_{CCAUX}$ | 1.8V 5% | | | | | |
| $V_{CCAUX\_IO}$ | | 1.8V 5% 2.0V 3% | 1.8V 5% 2.0V 3% | | 1.8V 5% 2.0V 3% | 1.8V 5% 2.0V 3% |
| $V_{CCO}$ | 1.2V - 3.3V 5% | | | | | 1.0V – 2.5V 5% 3.3V +3% / -5% |
| $V_{CCBATT}$ | Battery voltage 1.0V - 1.8V only for bitstream encryption, if unused connect to Vccaux or GND | | | | | |

- Note tolerance requirement variation between families

# Zynq PS and Transceiver Voltages

| | ZYNQ | | ARTIX 7 | KINTEX 7 / VIRTEX 7 | | UltraSCALE |
|---|---|---|---|---|---|---|
| Bank Name | 7010/15 /20 | 7030/45 /100 | GTP Transceivers | GTX Transceivers | | GTH Transceivers |
| $V_{CCPINT}$ | 1V @ 5% | | | | | |
| $V_{CCPAUX}$ | 1.8V @ 5% | | | | | |
| $V_{CCPLL}$ | 1.8V @ 5% | | | | | |
| $V_{CCO\_DDR}$ | 1.2V – 1.8V @ 5% | | | | | |
| $V_{CCO\_MIO}$ | 1.2V – 3.3V @ 5% | | | | | |
| $V_{MGTAVCC}$ | 1V @ 3% | | | | | |
| $V_{MGTAVTT}$ | 1.2V @ 2.5% | | | | | |
| $V_{MGTAVTTRCAL}$ | | 1.2V @ 2.5% | | 1.2V @ 2.5% | | |
| $V_{MGTVCCAUX}$ | | 1.8V @ 2.78% | | 1.8V @ 2.78% | | |
| $V_{CCADC}$ | 1.8V @ 5% | | | | | |
| $V_{REFP}$ | 1.2V @ 2.5% | | | | | |

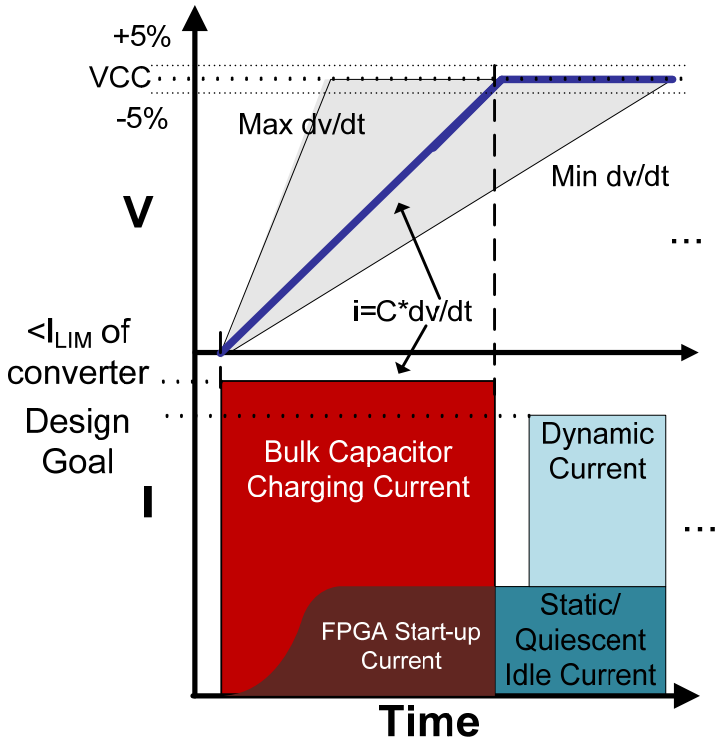
- Tie MGT power rails to GND if transceivers aren't used
- Tie $V_{CCADC}$ to $V_{CCAUX}$ if unused

# Supply Start-up and Sequencing

- Requirements for all rails
  - Monotonic rise
  - Ramp-Up
    - 0.2 to 50ms for 7 series and Zynq
    - 0.2 to 40ms for UltraScale
  - Sequencing
    - All 7 series and UltraScale share the same sequencing requirement by voltage type
    - Like voltages can be powered by the same supply
  - Logic Rails

    $V_{CCINT}$ ⇨ $V_{CCBRAM}$ ⇨ $V_{CCAUX}$ ⇨ $V_{CCAUX\_IO}$ ⇨ $V_{CCO}$
  - Zynq Processor Rails

    $V_{CCPINT}$ ⇨ $V_{CCPAUX/VCCPLL}$ ⇨ $V_{CCO\_MIO/DDR}$




- No sequencing between PS and PL inside Zynq

# Sequencing Continued

- Zynq PL supplies can be shut down to save power
  - Be sure to follow recommended start up and shut down sequencing

- Transceivers now have recommended sequencing

  $V_{CCINT}$ / $V_{MGTAVCC}$ ⇨ $V_{MGTAVTT}$

  - Not following recommendations can result in additional current draw at startup

  - $V_{CCINT}$ and $V_{MGTAVCC}$ can be powered at the same time

  - Either $V_{CCINT}$ or $V_{MGTAVCC}$ can come up first, as long as they both start before $V_{MGTAVTT}$

# Sequencing Continued

- Recommended power down sequence is reverse order of start up
- Shut-down sequencing more difficult than start-up
- For 7 Series devices, the following condition must be met to avoid damage

$T_{VCCO2VCCAUX}$ = time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$

$T_{VCCO2VCCAUX}$ = 500ms

One power cycle = startup + shutdown

- In most cases, natural discharge of a 3.3V Vcco rail and a 1.8V Vccaux rail will result in the delta voltage threshold of 2.625V never being violated
  - $i = C\frac{dv}{dt}; \quad i = 1A;\ dv = .675V\ (3.3V\ - 2.625V);\ dt = 500ms$
  - $C = i\frac{dt}{dv}; \quad C = 0.741\ F\ just\ to\ remain\ above\ 2.625V\ for\ 500ms$

# Xilinx XPower Estimator

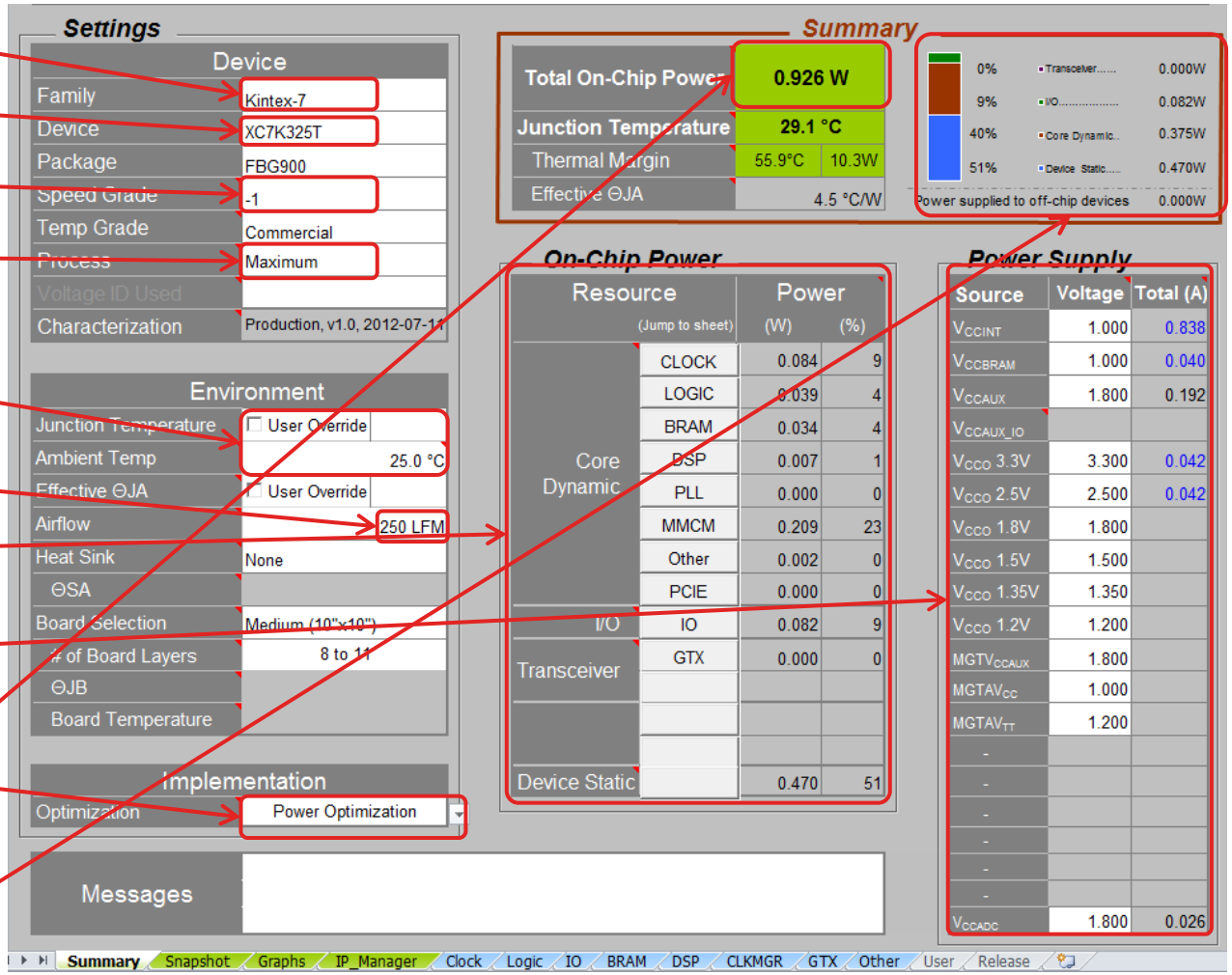

# Xilinx Power Estimation

- Pre-implementation (Pre PCB) – XPower Estimator (XPE)
  - Provides a power estimate based on your usage model
- Optimization – Vivado Power Optimization
  - Enables power saving features inside the FPGA
- Verification – Vivado Power Analysis
  - Provides power consumption figures based on your design

**XPE IS MOST IMPORTANT STEP FOR YOUR PCB DESIGN!**

# XPower Estimator (XPE)

- Family
- Part
- Speed Grade
- Process
- Calculated or Forced TJ
- Airflow
- Power by Resource
- Current by Supply
- Optimization
- Total On-Chip Power
- Summary of by Type

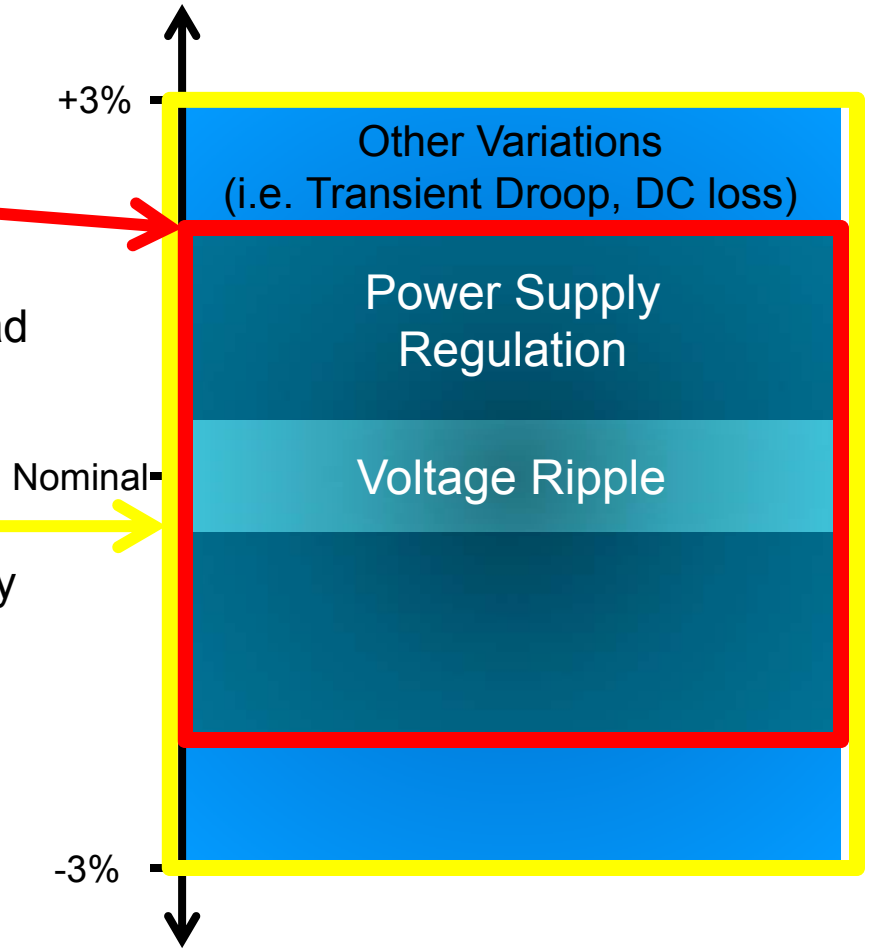


# Demo

# Power System Design

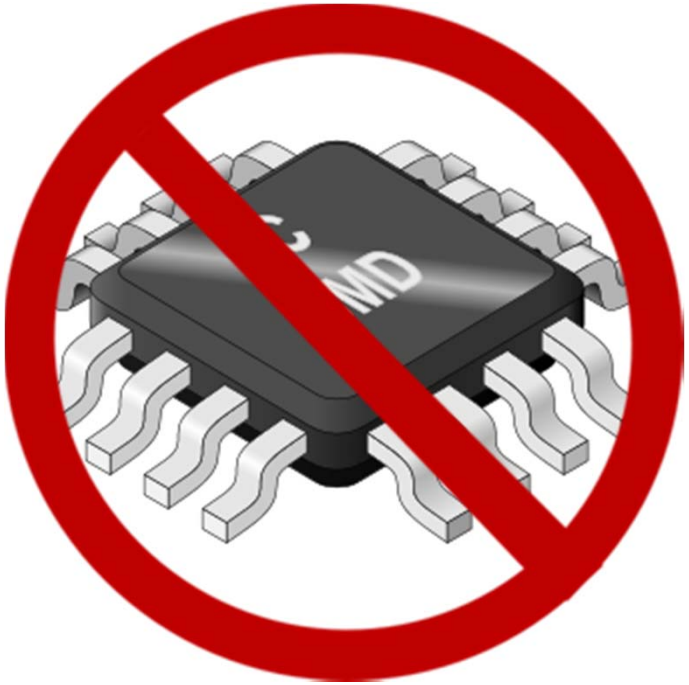

# Designing the Power System

- Power supply performance is considered under two operating conditions
  - Static
    - Operating conditions are fixed or changing gradually
      - Slow variations in input voltage, load current and temperature
    - Noise (voltage ripple) is considered under this condition
  - Dynamic
    - Operating conditions change relatively quickly
      - Sudden changes in load current referred to as load transients
- How well does the power supply regulate under these conditions?
- Diagram depicts an overall regulation accuracy requirement of 3%



# Would this part be a good choice?

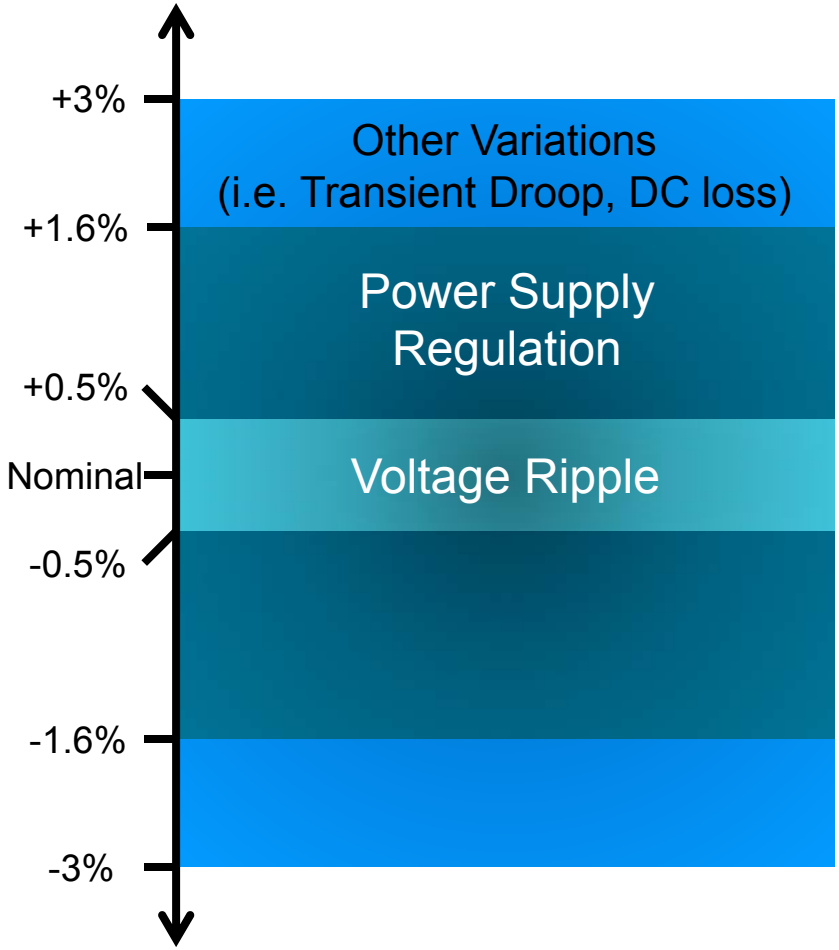
**LTC3414 - 4A, 4MHz, Monolithic Synchronous Step-Down Regulator**
**Features**
**High Efficiency: Up to 95%**
**4A Output Current**
**Low Quiescent Current: 64µA**
Low RDS(ON) Internal Switch: 67 milliOhm
Programmable Frequency: 300KHz to 4MHz
2.25V to 5.5V Input Voltage Range
±2% Output Voltage Accuracy
0.8V Reference Allows Low Output Voltage



This device would not be a good choice since the regulation accuracy is only 2%, leaving you with only 1% margin for all other regulation error sources

# 3% Design Example

- Meeting the tolerance specification of ± 3%




**Example:** $V_{CCINT}$ = 1.0V @ 3A

| | |
|---|---|
| Regulator | |
| - reference | ± 1.000% |
| - line regulation | ± 0.010% |
| - load regulation | ± 0.005% |
| - feedback Rs | ± 0.080% |
| Voltage Ripple | ± 0.500% |

Other Variations..±1.4% (14mV)

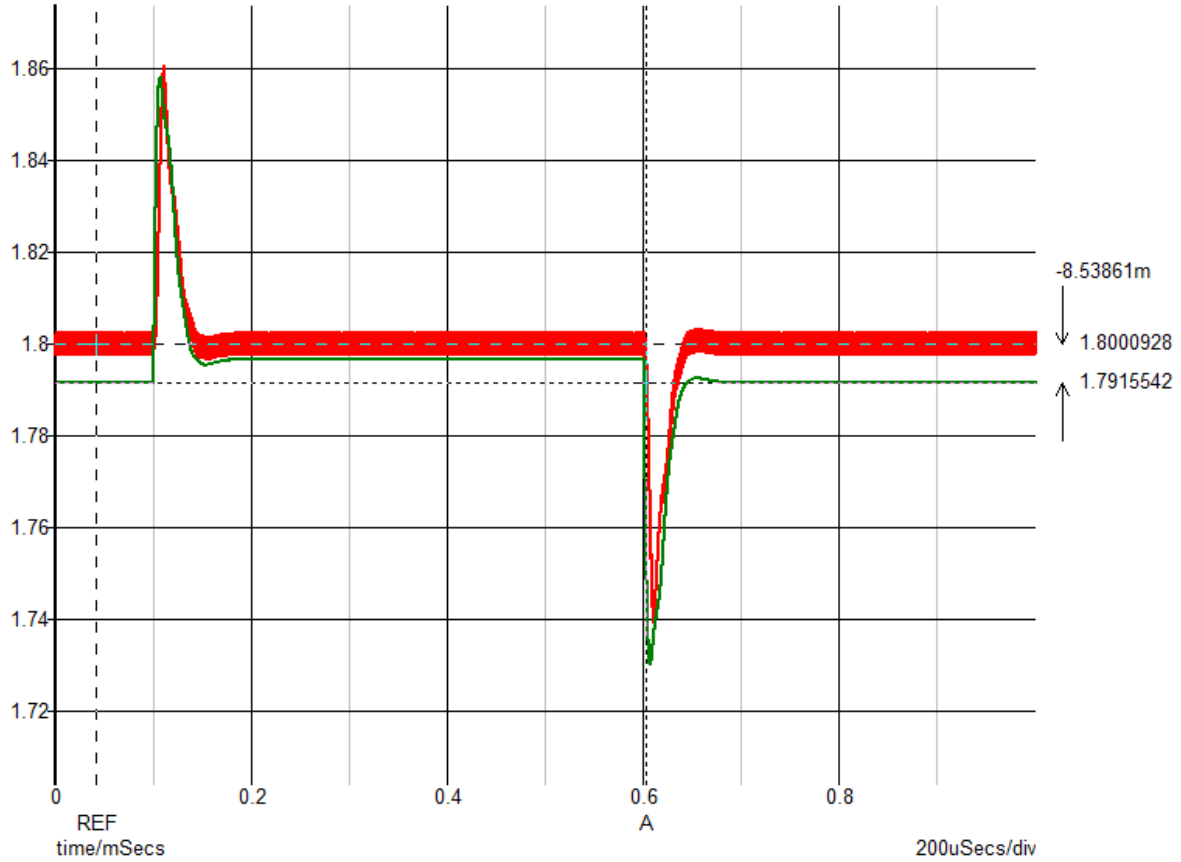
**DC Loss Examples:**

6A Chip Ferrite
Bead RDC……0.01Ω (30mV)

1 oz copper, 1/2” trace, ¼” wide
……...0.001Ω (3mV)

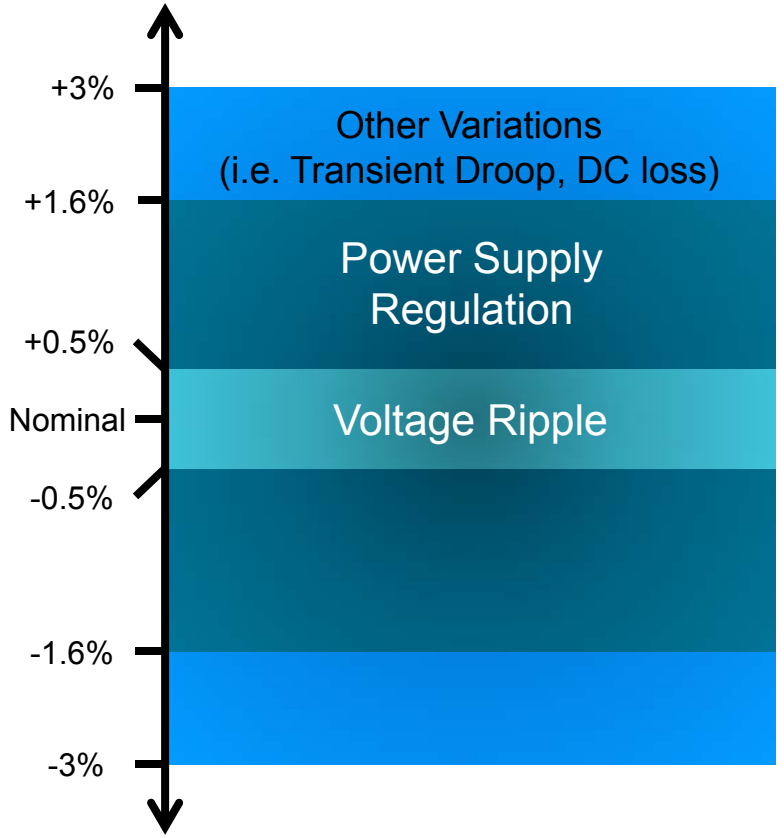
# Ferrite Bead Loss Example

- ADP5050 Channel 1 ADIsimPE Simulation
  - 220nH/5mohm filter bead
  - Red shows pre filter
  - Green post filter
  - Noise is reduced from 5mV to <100uV
  - Voltage drop is 8.5mV due to 1.8A load



# Meeting the 3% Tolerance

- Use high quality power regulators
  - ≤ 1% regulation
  - High quality capacitors*
- Understand set resistor error
  - Consider fixed output regulators
  - Choose high precision feedback resistors (0.1% or better) with adjustable regulators+
  - $error \cong \left(1 - \frac{Vref}{Vout}\right) \times \pm 2 \times tolerance$
- Minimize voltage ripple (Noise)
  - Optimized power stage design
- Minimize DC loss
  - Use wide tracks/planes for PCB
  - Locate power supply next to FPGA
  - Be careful with current sense resistors and filters (ferrite beads)
  - Remote sense
- Minimize transient droop

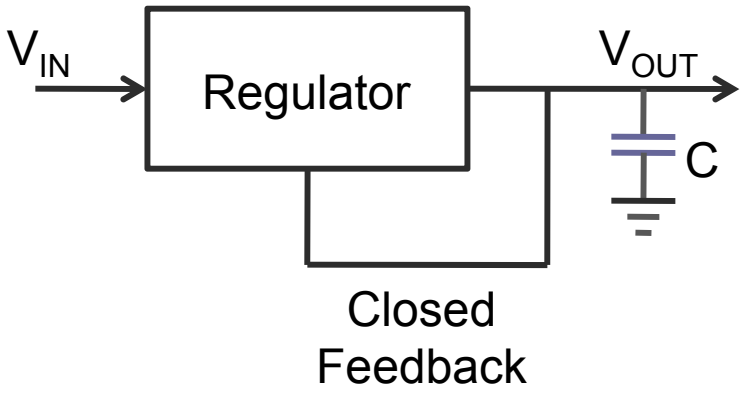


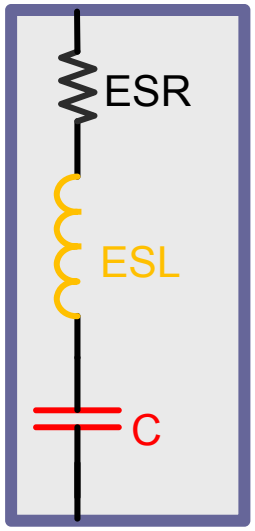

+ TI app note SLVA423 for details on this equation
www.ti.com/litv/pdf/slva423

* Maxim app note 5527 on ceramic cap variations
www.maximintegrated.com/en/app-notes/index.mvp/id/5527

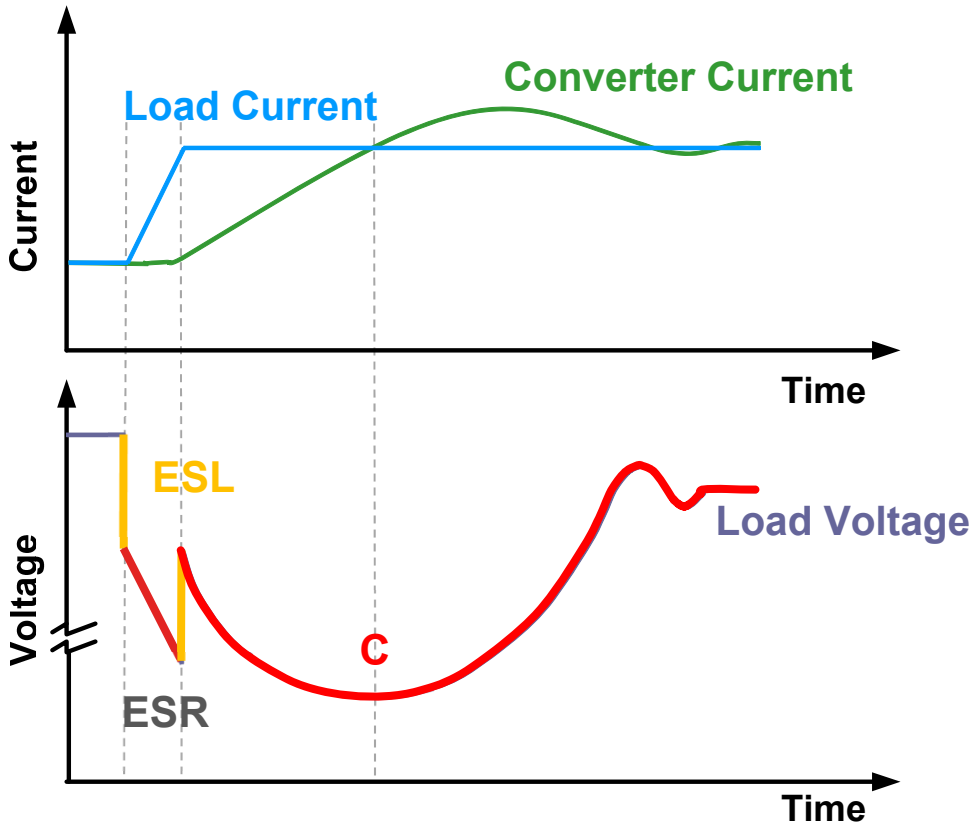
# Load Transient Model

- Load Transients



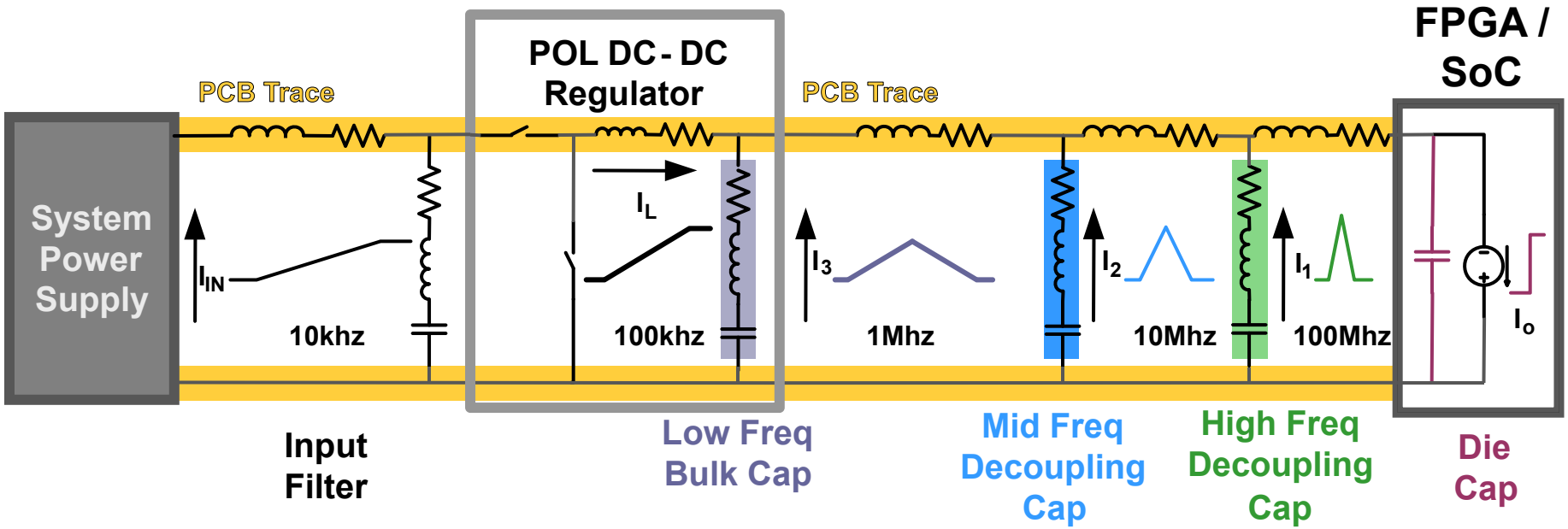




Capacitor
Model



# Decoupling Network Breakdown

- Decoupling Network



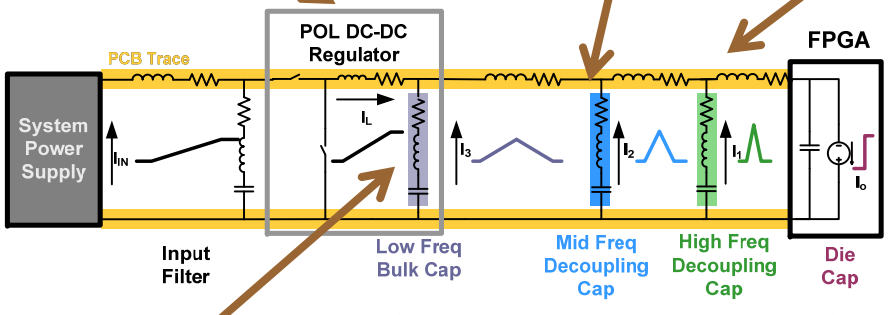
# Bringing it all together

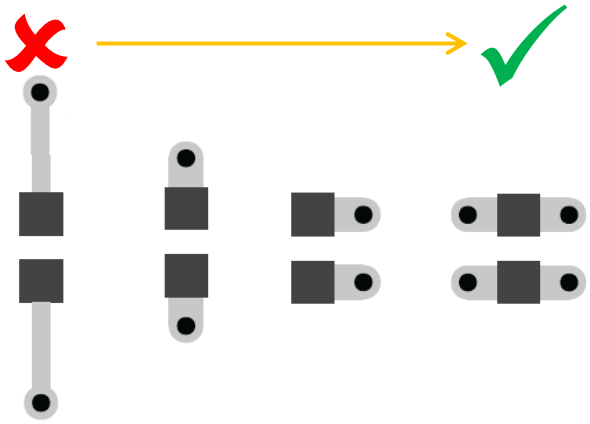
- Minimizing Transient Voltage Droop

Proper layout of capacitor landing pad
(See Xilinx XAPP623)

High bandwidth voltage converter

Wide and short traces



Complete and effective decoupling network

Sufficient bulk capacitance

Good quality, low ESR capacitors
Ceramic X5R and X7R dielectrics are great choices

# Power System Considerations

- Decoupling Recommendations
  - Follow PCB and Pin Planning Guides
    - UG483 and UG583 for 7 Series and UltraScale
    - UG933 for Zynq 7000
    - UG476 and UG576 for 7 series and UltraScale transceivers

**Required PCB Capacitor Quantities per Device: Kintex-7 Devices**

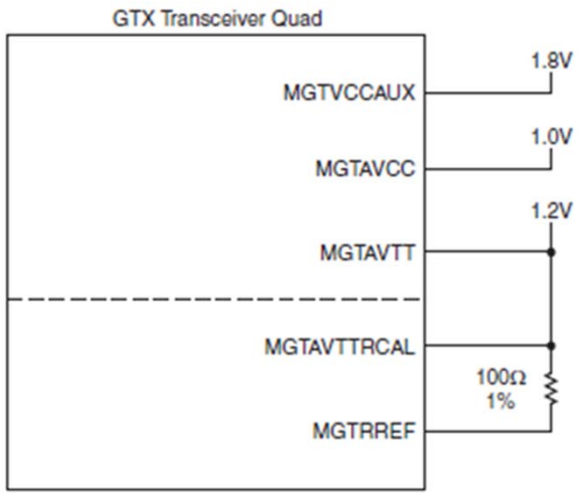
| Package | Device | $V_{CCINT}$ | | | $V_{CCBRAM}$ | | | | $V_{CCAUX}$ | | $V_{CCAUX\_IO}$ per Group[3] | | | $V_{CCO}$ Bank 0 | $V_{CCO}$ all other Banks (per Bank) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 680 µF | 330 µF | 4.7 µF | 660 µF | 330 µF | 100 µF | 4.7 µF | 47 µF | 4.7 µF | 100 µF | 47 µF | 4.7 µF | 47 µF | 100 µF |
| FBG484 | XC7K70T | 0 | 1 | 0 | 0 | 0 | 1 | 2 | 2 | 3 | N/A | N/A | N/A | 1 | 1 |
| FBG484 | XC7K160T | 0 | 2 | 0 | 0 | 0 | 1 | 3 | 2 | 3 | N/A | N/A | N/A | 1 | 1 |
| FBG676 | XC7K70T | 0 | 1 | 0 | 0 | 0 | 1 | 2 | 2 | 3 | 0 | 0 | 0 | 1 | 1 |
| FBG676 | XC7K160T | 0 | 2 | 0 | 0 | 0 | 1 | 3 | 3 | 4 | 0 | 0 | 0 | 1 | 1 |
| FBG676 | XC7K325T | 0 | 3 | 5 | 0 | 0 | 2 | 5 | 3 | 4 | 0 | 0 | 0 | 1 | 1 |
| FBG676 | XC7K410T | 0 | 5 | 10 | 0 | 1 | 0 | 9 | 3 | 4 | 0 | 0 | 0 | 1 | 1 |

*Table 5-4:* **GTX/GTH Transceiver PCB Capacitor Recommendations**

| Quantity Per Group | | | Capacitance (µF) | Tolerance | Type |
|---|---|---|---|---|---|
| MGTAVCC | MGTAVTT | MGTVCCAUX | | | |
| 1 | 1 | 1 | 4.70 | 10% | Ceramic |

# Transceiver Power Supply Design

- High speed transceivers (GTP, GTX, GTH)
  - Analog I/Os and are sensitive to power supply noise
    - Noise can result in increased jitter at the TX and reduced jitter tolerance on the RX
  - Traditionally only linear regulators were recommended
  - Switching supplies are acceptable if designed for low noise/ripple (<10mVpk-pk, 10khz-80Mhz)

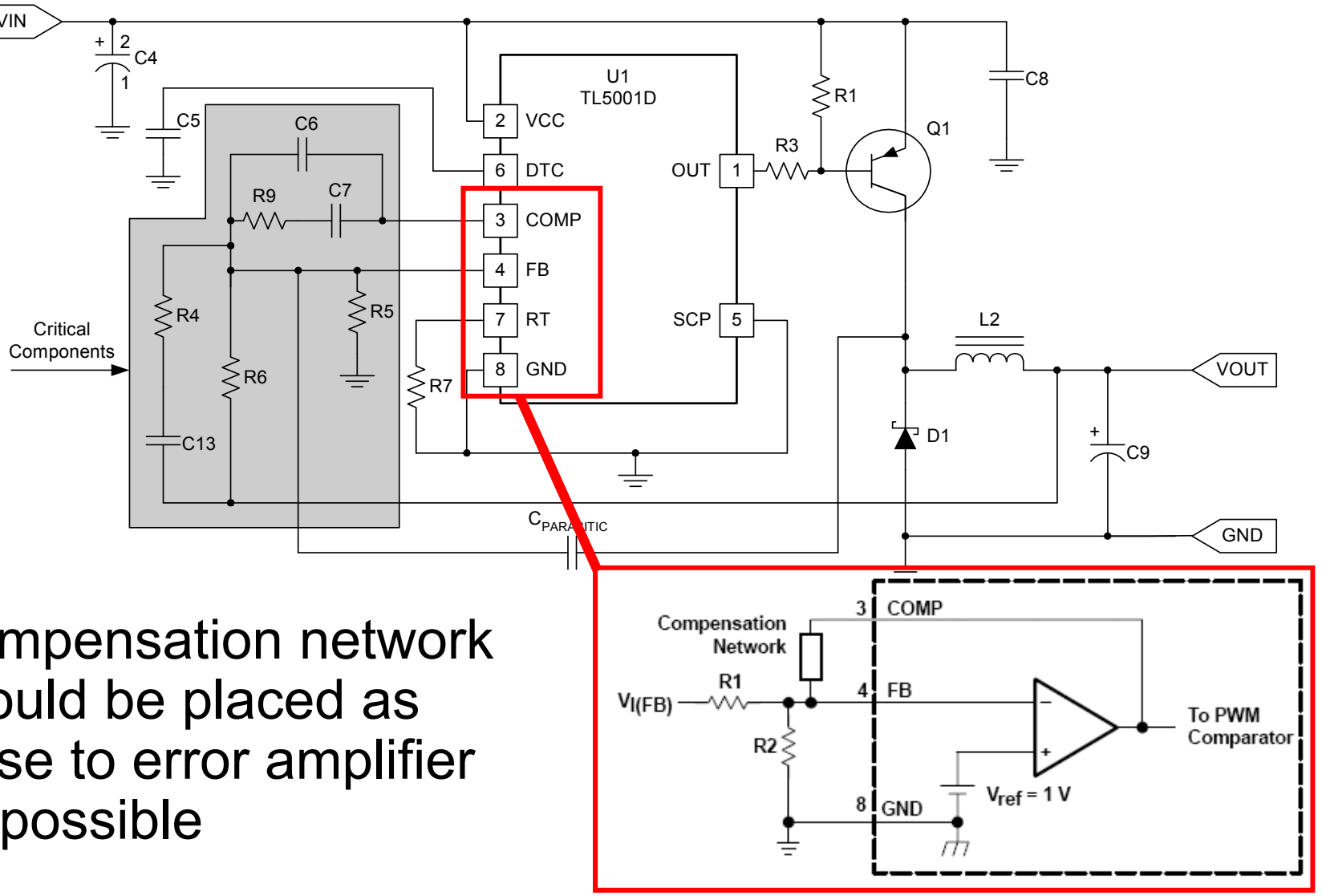



| | Linear Regulators | Switching Regulators |
|---|---|---|
| Advantages | Low Noise | Efficient over a large range of operating conditions |
| | Simple Design | |
| Disadvantages | Can be inefficient<br>Eff ≈ Vout/Vin | Switching Noise |
| | | Complex design |

# Transceiver Power Supply Design

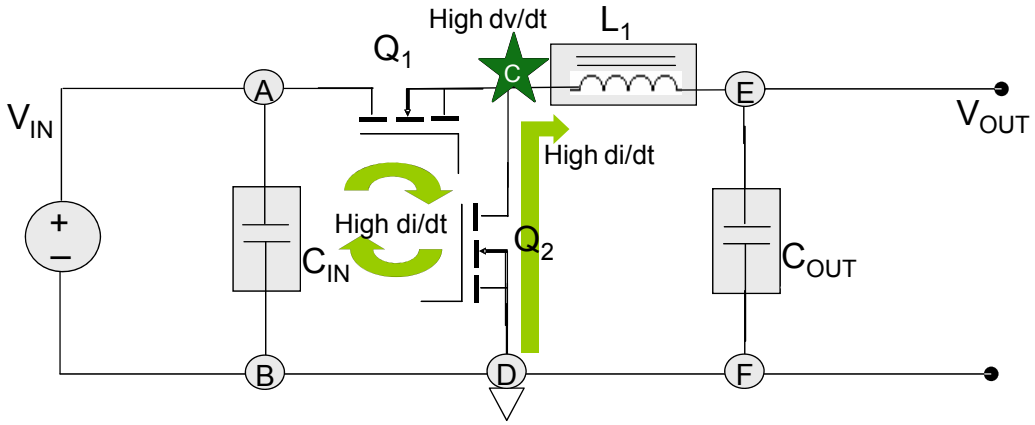
- Avoid coupling from noise sources
  - Place regulator as close as possible to transceiver power pins
  - Avoid routing digital traces in the vicinity of analog power regulator circuits
  - Avoid routing digital traces adjacent to analog power planes
- Follow the appropriate design guides
  - Xilinx 7 Series FPGAs GTX Transceivers UG476
  - Xilinx UltraScale GTH Transceivers UG576
- Minimize switching regulator noise
  - Use additional filtering
    - Such as ferrite beads or linear regulator
  - Use dedicated regulators
  - Properly layout the switching regulator to minimize noise and EMI

# Layout Guidelines – Compensation Network

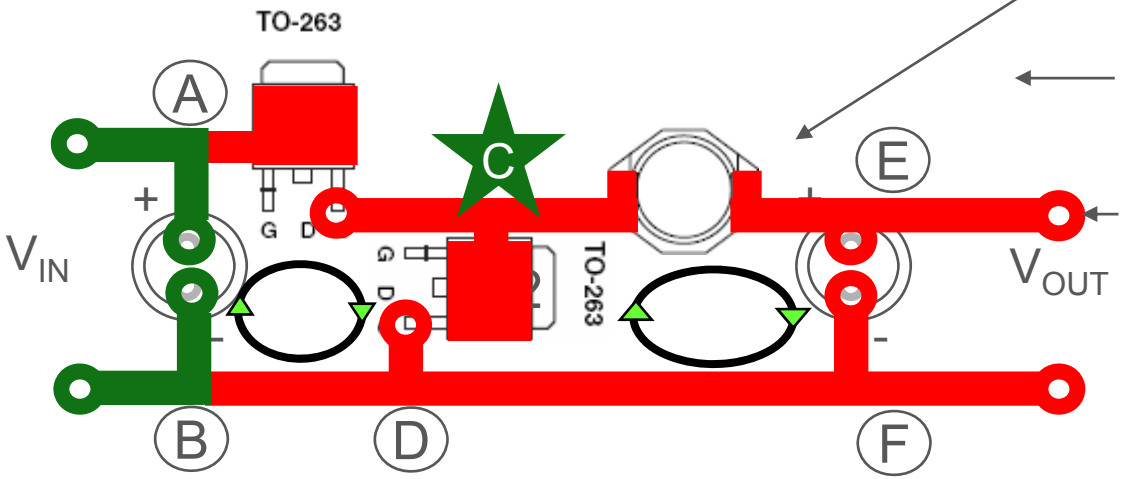



- Compensation network should be placed as close to error amplifier as possible

# Layout Example 1




From the Identification of the High Current Paths …




1. Place Components (like above)

2. Identify the voltage nodes

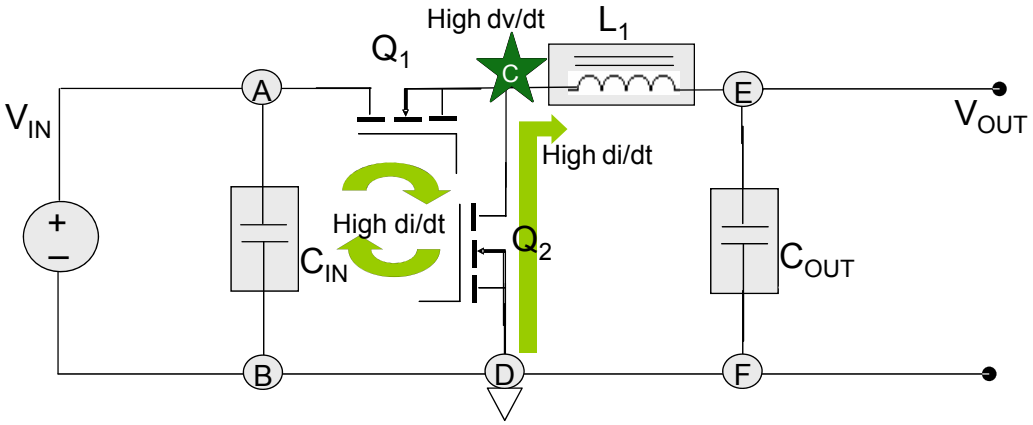
3. Estimate the routing paths

4. Identify large inductive loops in the Red and Green paths

This circuit will generate a lot of Q1 and Q2 switching noise…

Example 1. Layout like the above schematic …

# Layout Example 2



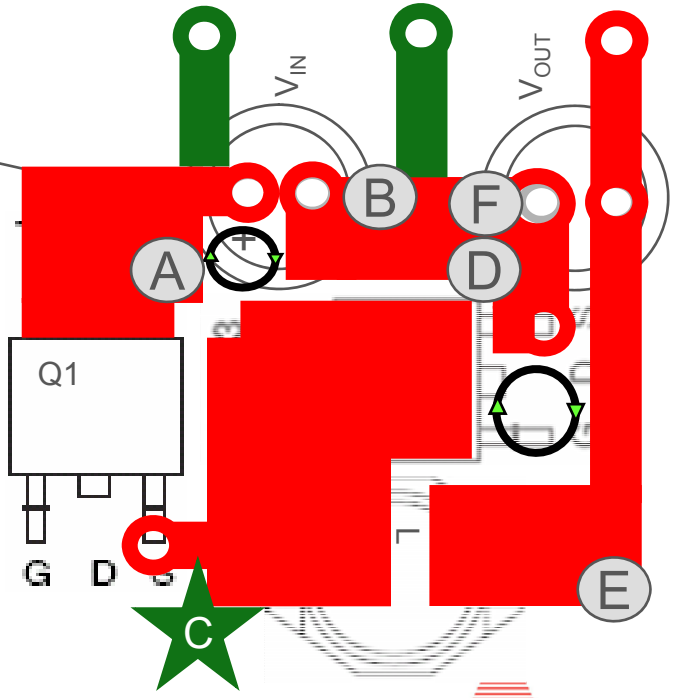

Identify of the High Current Paths on the Schematic …

1. Place Components (To keep traces short)

2. Identify the voltage nodes (Notice B,D,&F are adjacent)

3. Estimate the routing paths (Use Blocks)

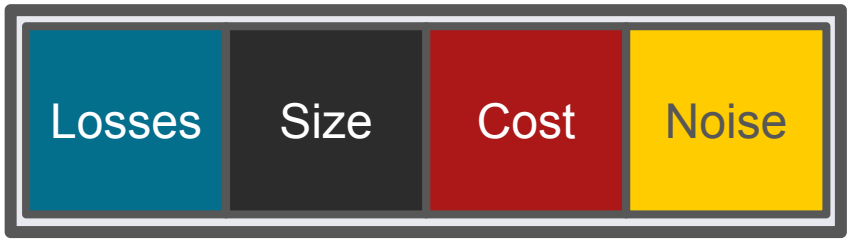
4. Identify large inductive loops in the Red and Green paths



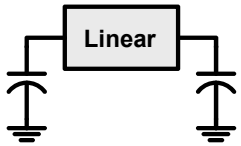

With the proper layout the switching noise from Q1 and Q2 is greatly reduced …..

# Topologies

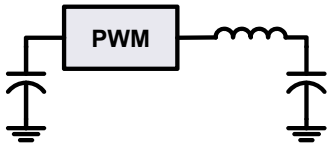
- No perfect solution
  - 100% Efficient, Zero Noise, Zero Size, No Effort, Zero Cost
- Constant tradeoff
  - Efficiency, noise, size, design effort, cost, and specs




**Linear Regulator**




**Switching Mode Power Supply (SMPS)**




**Power Module**

**Integrated Power Module**

**Power Management IC - PMIC**

Broadly used term to describe multi function power devices

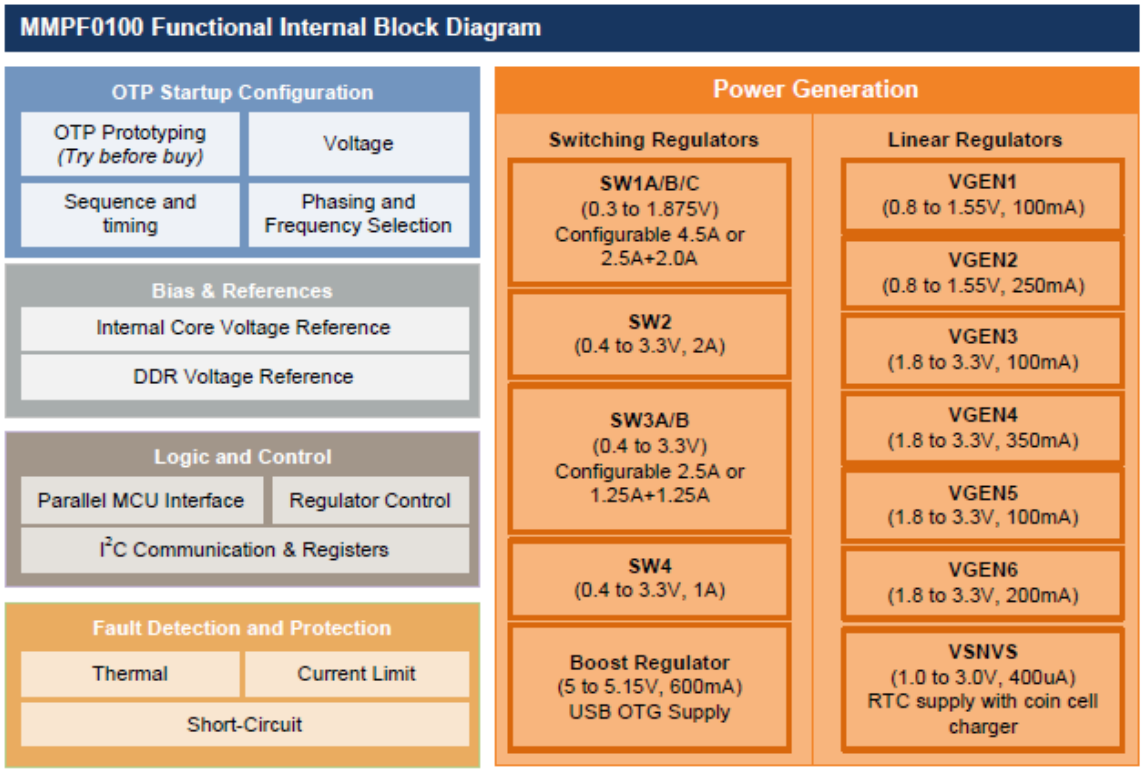
# Power Management IC's

- Often designed around specific target devices
  - FPGAs, MCUs, MPUs, etc
  - Although preset to certain parts, can be used in a wide variety of applications

- Typically multiple outputs
  - Additional features often included
    - Telemetry
    - Reset control
    - Watchdog
    - RTC

# Freescale PMIC

- MMPF0100
  - i.MX6 companion device
  - Up to 6 buck
  - 1 boost
  - 6 LDO
  - References
  - RTC
  - Fault detection

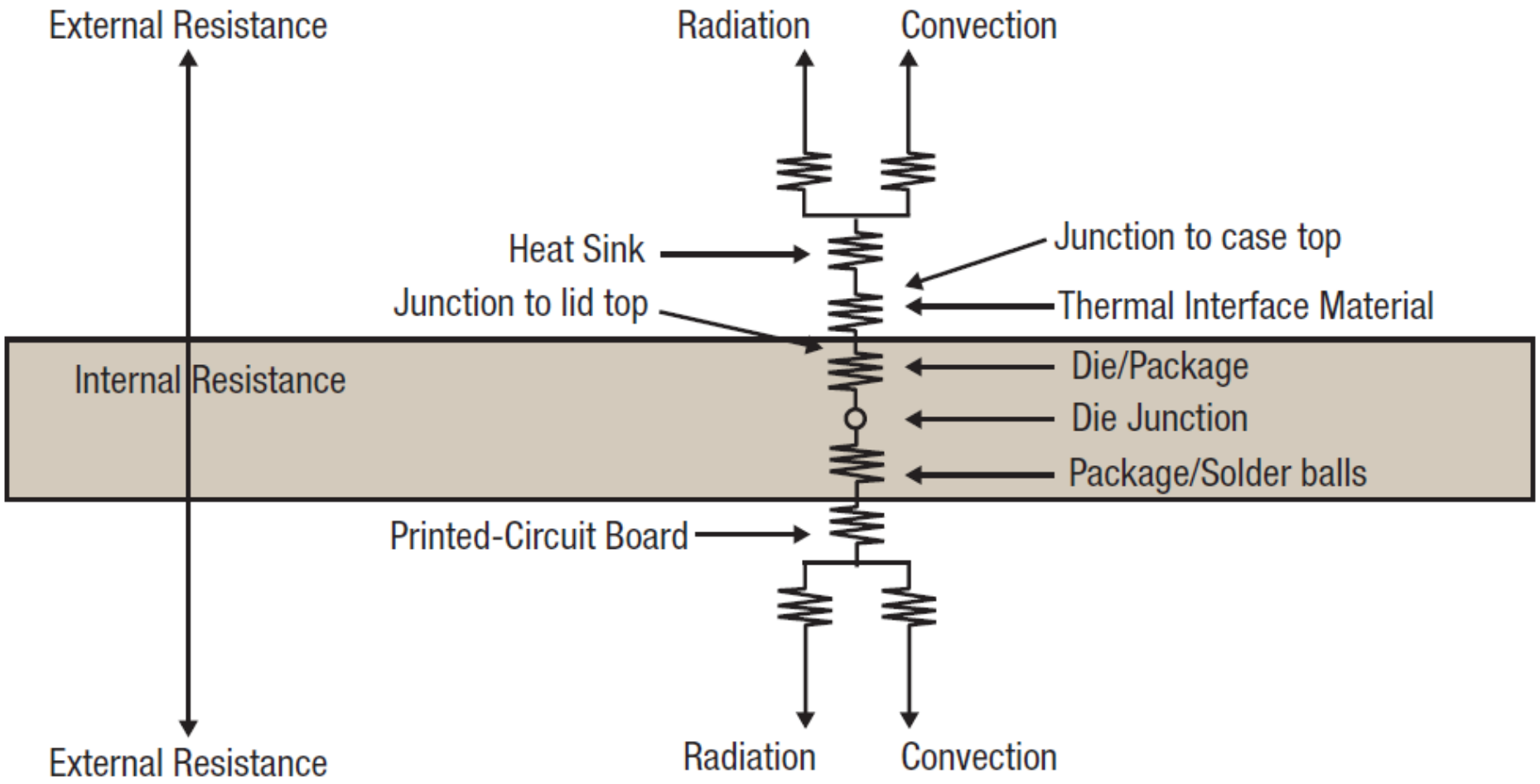


# Thermal Design


# Thermal Effect on components

- Inductors
  - As temperatures rise components lose their magnetic properties
- Capacitors
  - Capacitance values can change over temp
  - Different chemistries have different properties
- IC's often draw more current at higher temperatures
  - Temperature can effect reference accuracies and analog measurements

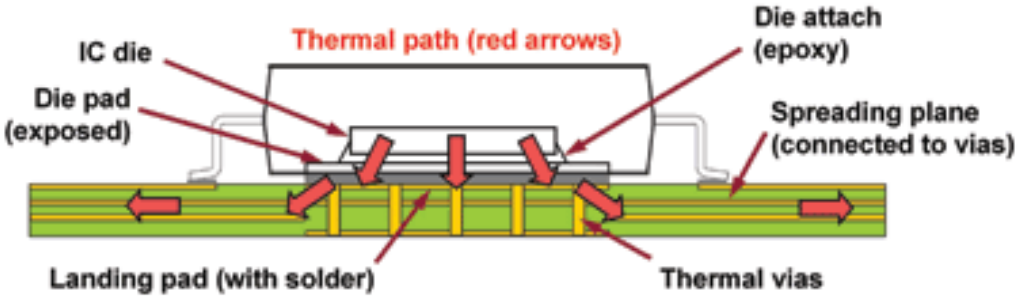
# Thermal Impedance Model



# Heat Transfer to PCB

- 3 elements
  - Junction to pins / thermal pads
  - Pins / thermal pads to PCB
  - PCB to ambient

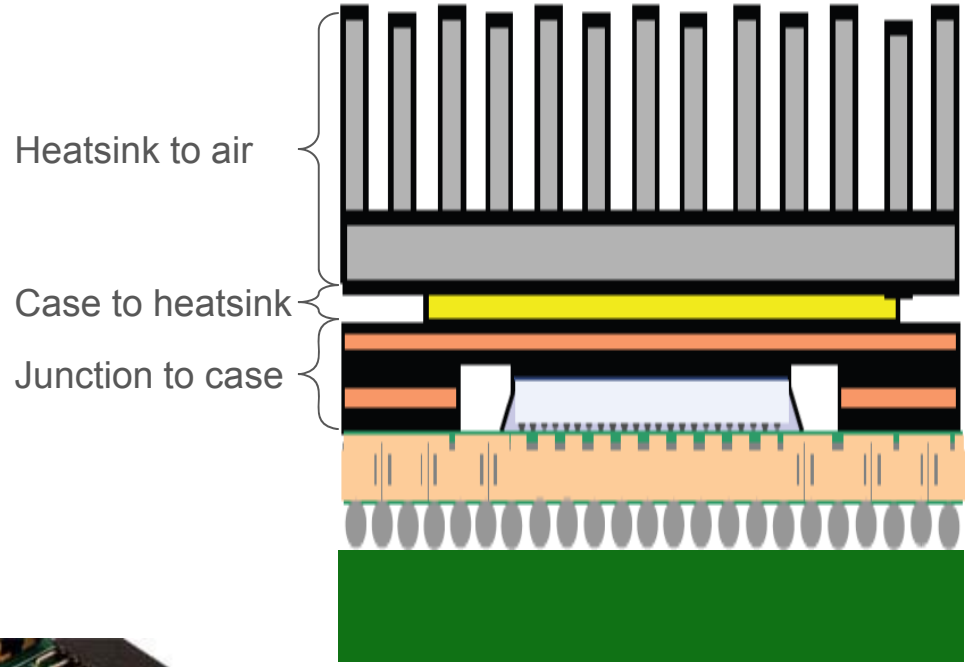
- PCB copper planes provide thermal relief
  - Better dissipation
    - Heavier copper weight
    - More planes
    - Thermal vias

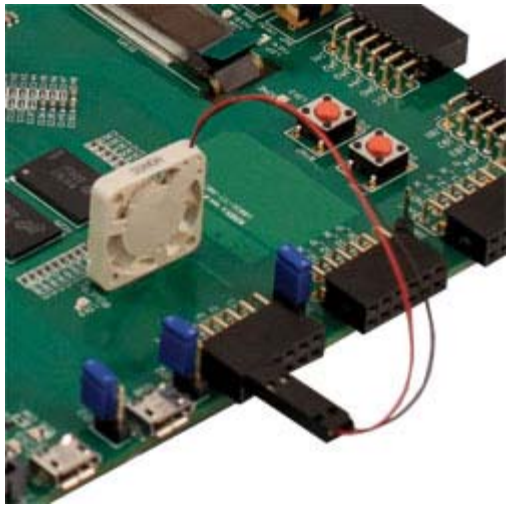



- Use vias without thermal reliefs

# Heat Transfer to Ambient

- 3 elements
  - Junction to case
  - Case to ambient / heatsink
  - Heatsink to ambient
- Effectiveness greatly increased through the use of airflow / fan



# Total Dissipation

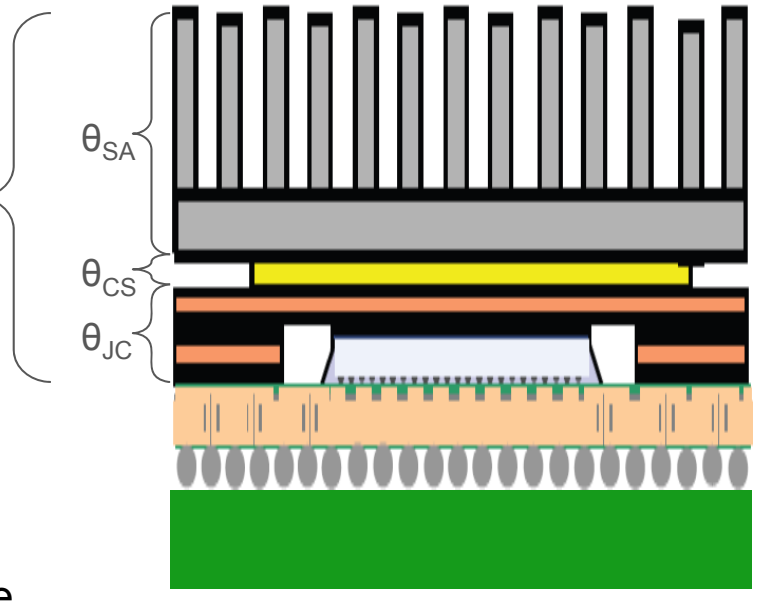
- Effectiveness dictated by the cumulative thermal resistance
  - Both IC through PCB and IC through case / heatsink
- Appropriate thermal management can greatly reduce operating temperatures increasing system reliability and lifespan
  - Thermal overload conditions can cause device protection activation, reset or failure

# MicroZed Design Example - 7010

Junction to Ambient = Junction to case + case to sink + sink to air
Desired Junction to Ambient = (max junction temp – max ambient) / chip power

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = (T_J - T_A)/Q$$

$T_J$ = 100ºC (max junction temp)
$T_A$ = 85ºC (max operating ambient)
$Q_{7010}$ = 2.6W (power dissipated by part – XPE)
$\theta_{CS}$ = 0.25ºC/W (Thermal impedance of adhesive)
$\theta_{JC\_7010}$ = 4.52ºC/W (Thermal impedance of FPGA)




http://www.xilinx.com/cgi-bin/thermal/thermal.pl

Rearrange equation to solve for heatsink impedance

$$\theta_{SA} = (T_J - T_A)/Q - \theta_{CS} - \theta_{JC}$$

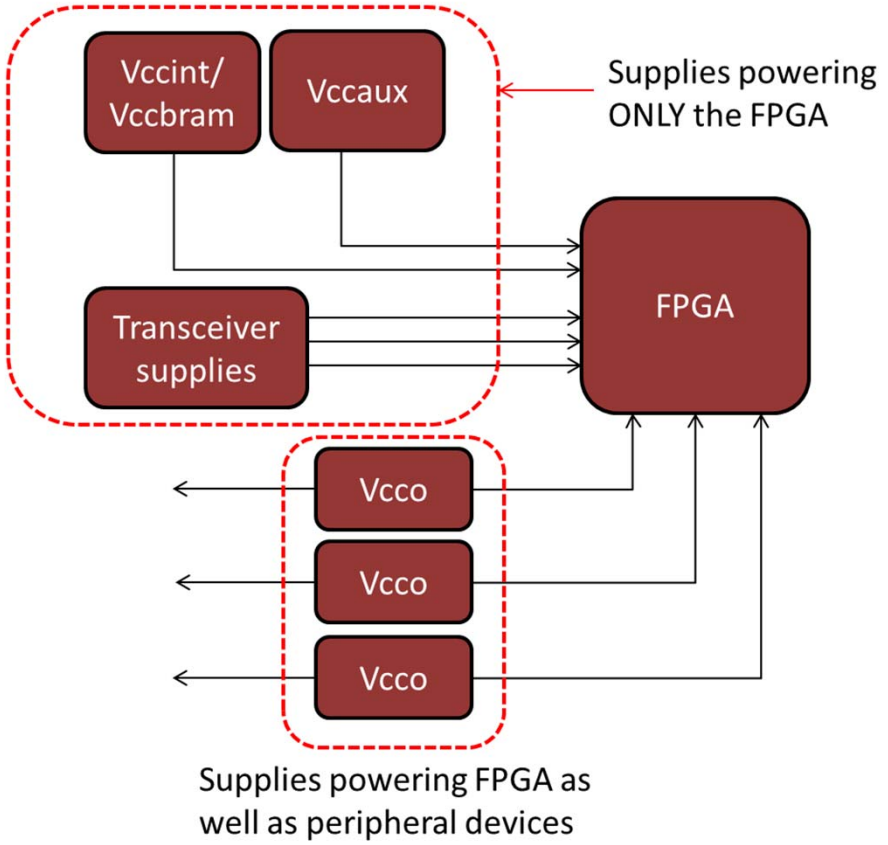
$$\theta_{SA} = (100ºC - 85ºC)/2.6W - 0.25ºC/W - 4.52ºC/W$$

$\theta_{SA}$ = 0.99 ºC/W – you must select a heatsink that will dissipate at least 0.99 ºC/W

# Design Resources Examples and Tools


# Xilinx Power Design Cookbook

- Get a head start on your power architecture design
  - Block diagram, schematic and BOMs for over 40 design examples
  - Expanding content

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ANALOG DEVICES

Texas Instruments

www.em.avnet.com/XilinxPowerDesigns

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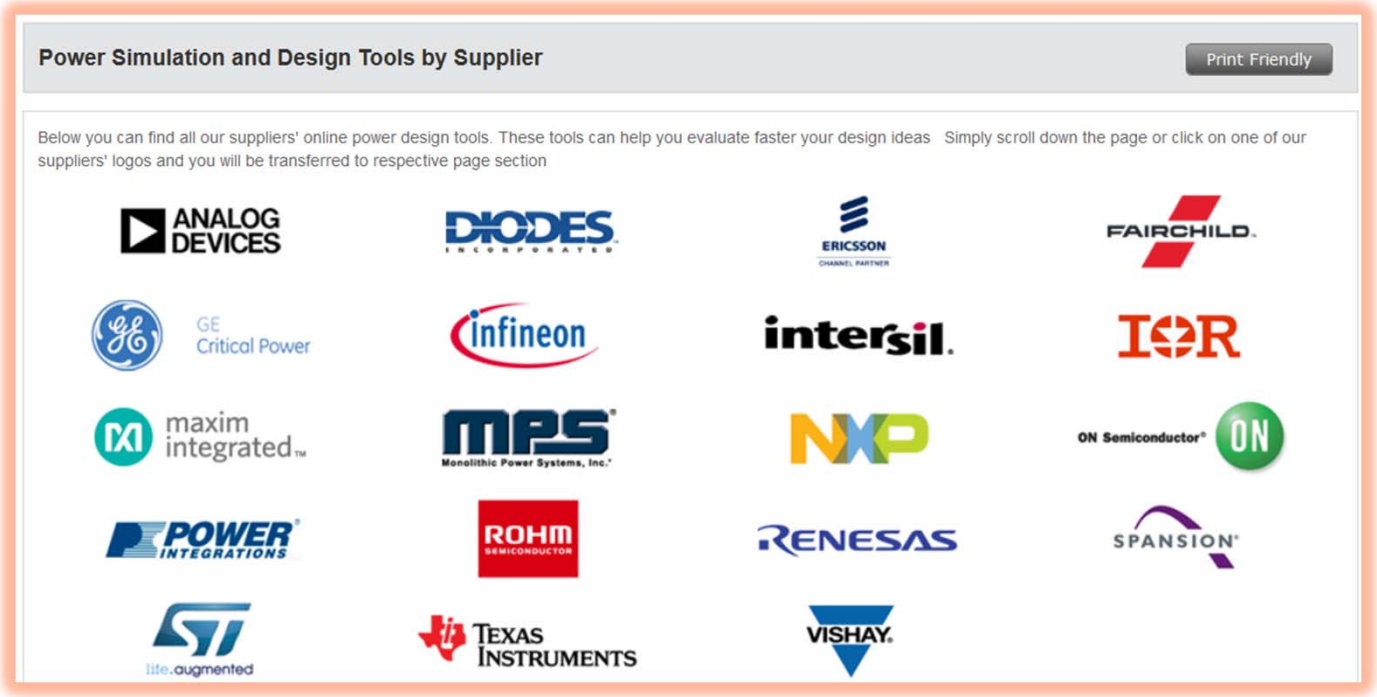
# Power Design Tool website

- Comprehensive collection of available design tools from supplier partners




www.em.avnet.com/PowerDesignTools

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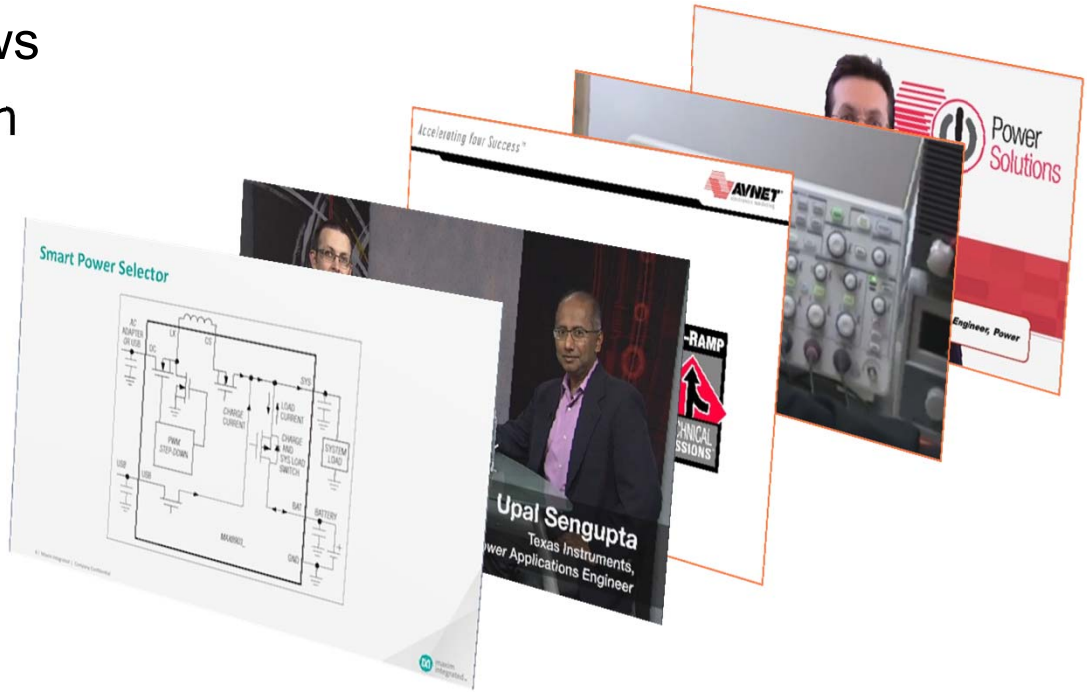
# Power Solutions Video Series

- Ongoing video series addressing a wide variety of topics related to power supply design
  - Regular content additions
    - Technology overviews
    - Component selection
    - Testing and more




Power Solutions

www.youtube.com/AvnetDesign

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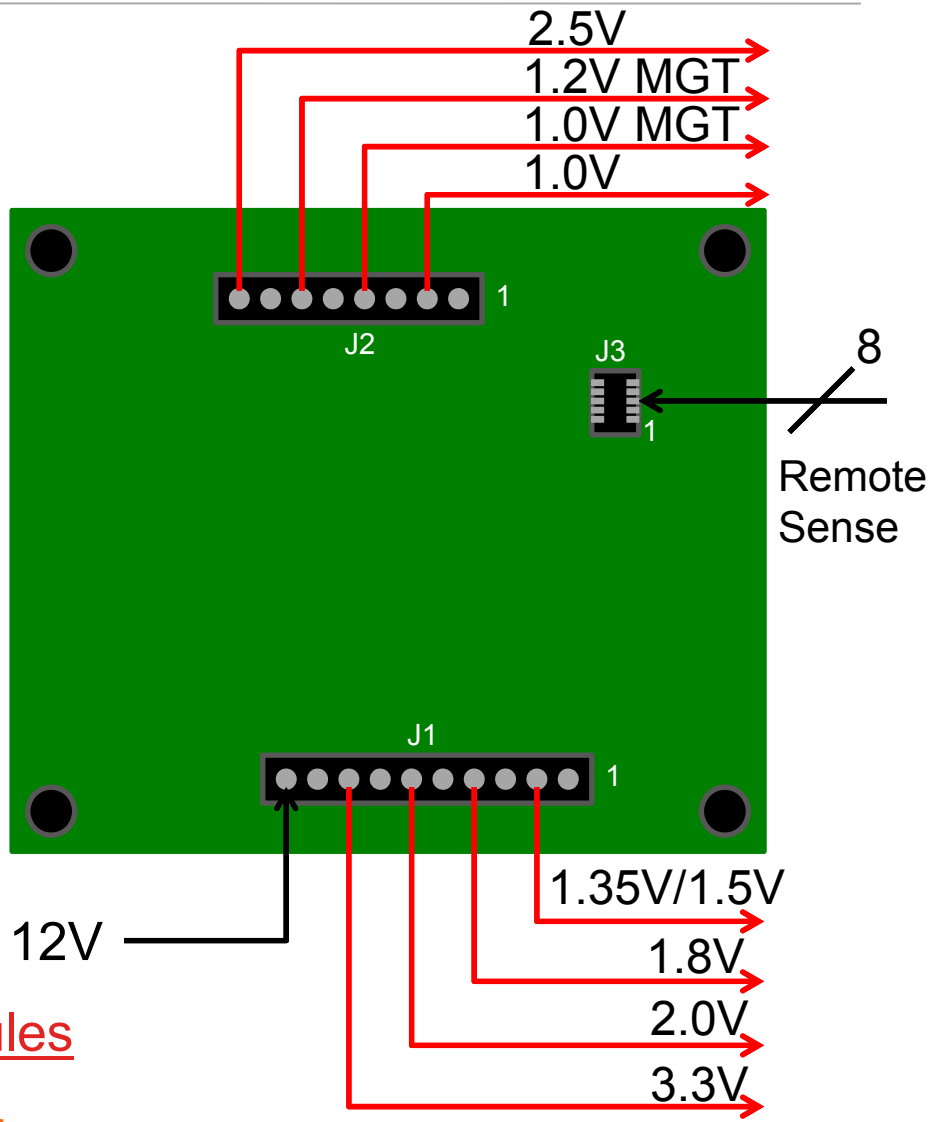
# Mini Module Plus Power Module

- Designed to meet the footprint and pinout shown
- Remote sense used on each board
- Low impedance, high current Samtec HPM / HPF headers and sockets chosen to minimize conduction losses
- 2 power headers used to simplify layout and routing
- Supports
  - Mini Module Plus development kit
  - Zynq Mini-ITX development kit
  - Your custom designs




www.em.avnet.com/avnetpowermodules

Xilinx fest

samtec

AVNET

# Avnet Power Modules

| Xilinx power bank / FMC Voltage | Voltage (V) | Max Current (A) | Tolerance |
|---|---|---|---|
| Vccint/Vccbram | 1 | 6 | 3.00% |
| Vcco | 1.5 / 1.35 | 4 | 5.00% |
| Vccaux/Vccaux_io/Vccadc Vcco/MGTVccaux | 1.8 | 6 | 5.00% |
| Vccaux_io | 2 | 2 | 3.00% |
| Vcco | 2.5 | 8 | 5.00% |
| Vcco | 3.3 | 8 | 5.00% |
| MGTAVcc | 1 | 6 | 3.00% |
| MGTAVtt/MGTAVTTrcal | 1.2 | 4 | 2.50% |

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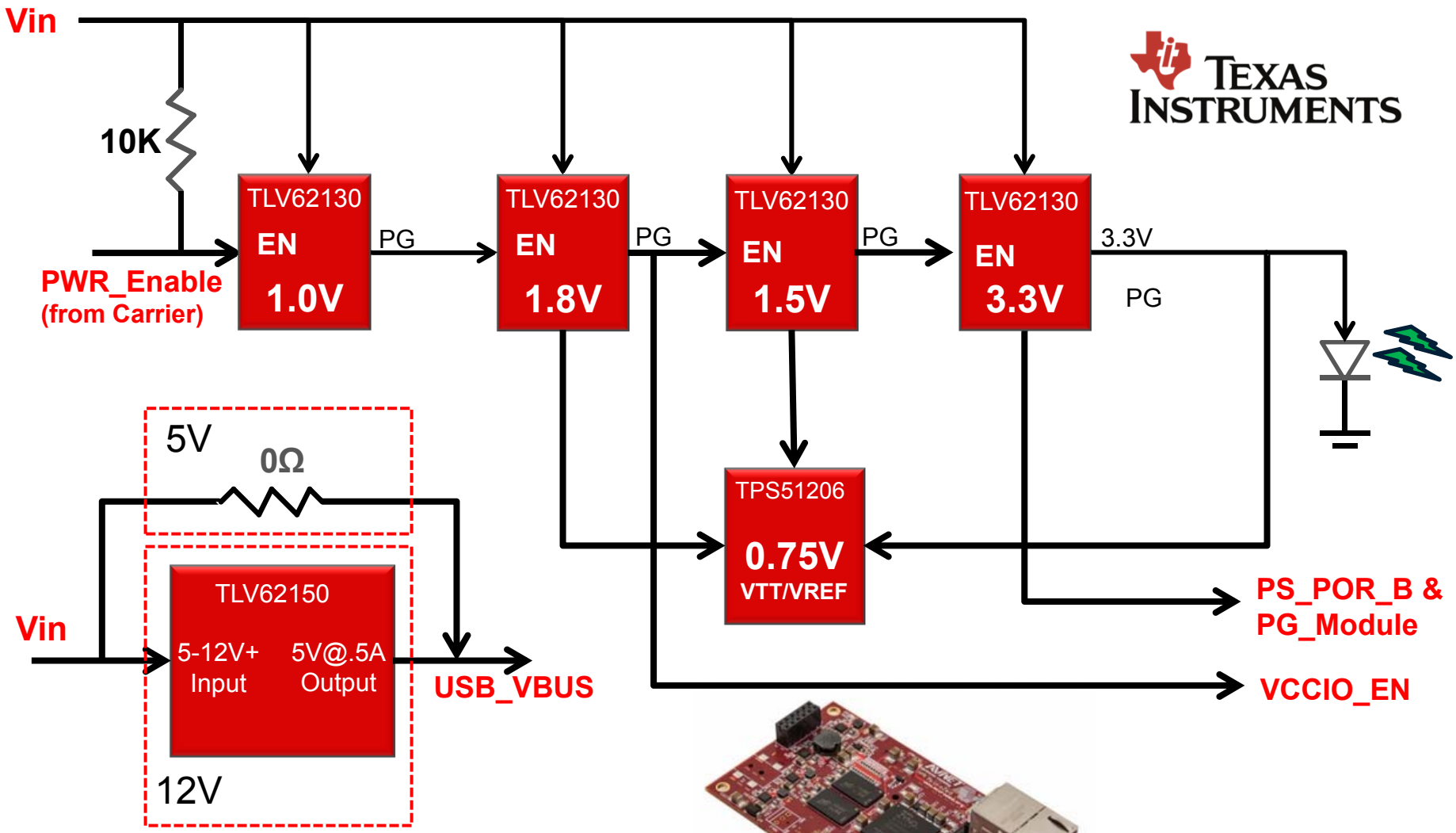
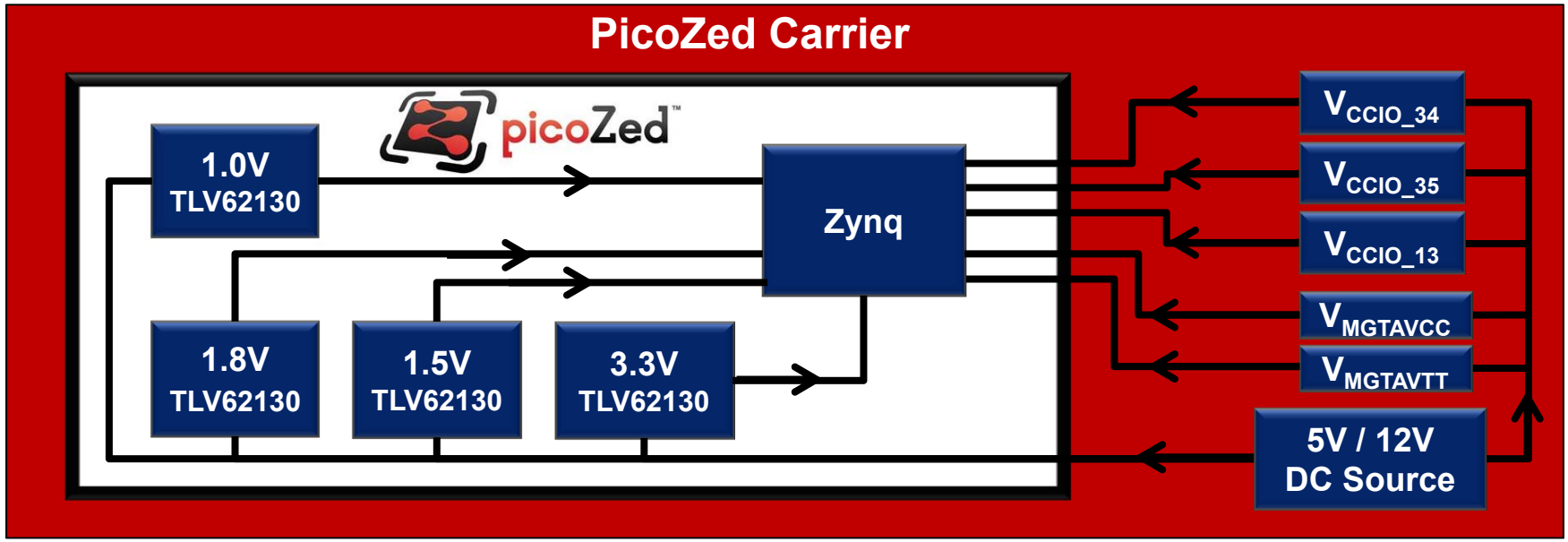
# MicroZed TI Power Block Diagram




# PicoZed Power Architecture




- PicoZed based on MicroZed
  - TI power architecture supports Vin 5-12V
  - 3 independent banks powered by carrier
  - 2 transceiver rails powered by carrier

picoZed™

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# TI WEBENCH® tools

1. Choose a part

Enter specifications

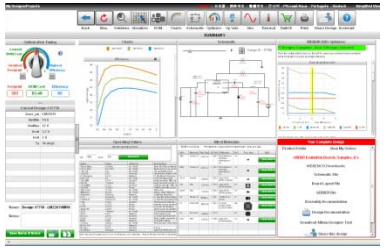
Select solution

**WEBENCH Visualizer**

**WEBENCH Optimizer**

Optimize for footprint, price and efficiency; use graphs to see design

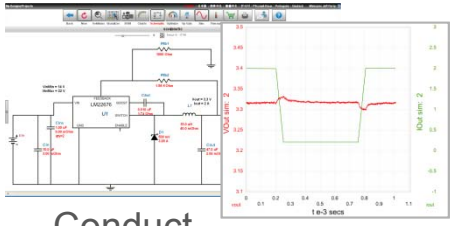
2. Create a design



**WEBENCH Create**

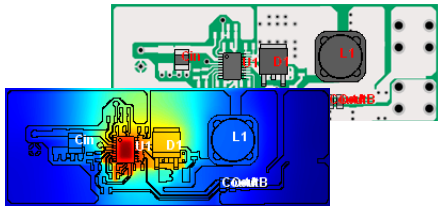
View schematic, change BOM and view key operating values

3. Analyze a design



Conduct electrical analysis

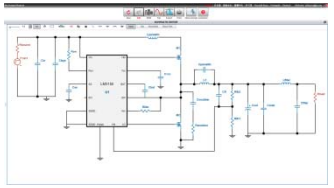
**WEBENCH Esim**



Generate layout/ thermal analysis

**WebTHERM**

4. Edit



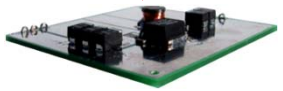
Change schematic/ electrical analysis

**WEBENCH Editor**

5. BuildIt!

**WEBENCH Export**

Mentor Graphics Altium cadence DESIGNSPARK



Design prototype

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**www.ti.com/webench**

**www.ti.com/tidesigns**

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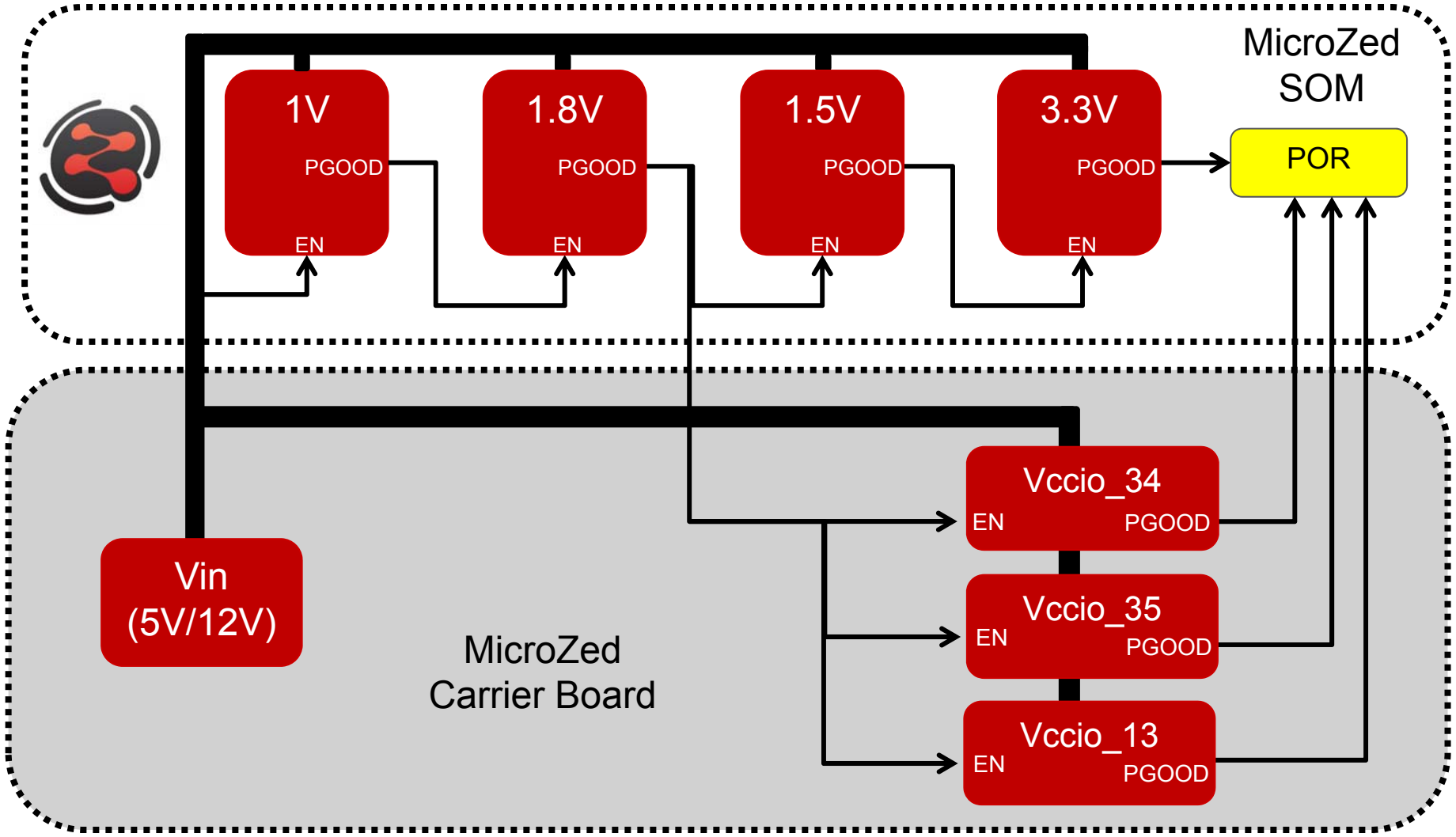
# MicroZed / Carrier Power Block



# Maxim Integrated MicroZed FMC Carrier Power

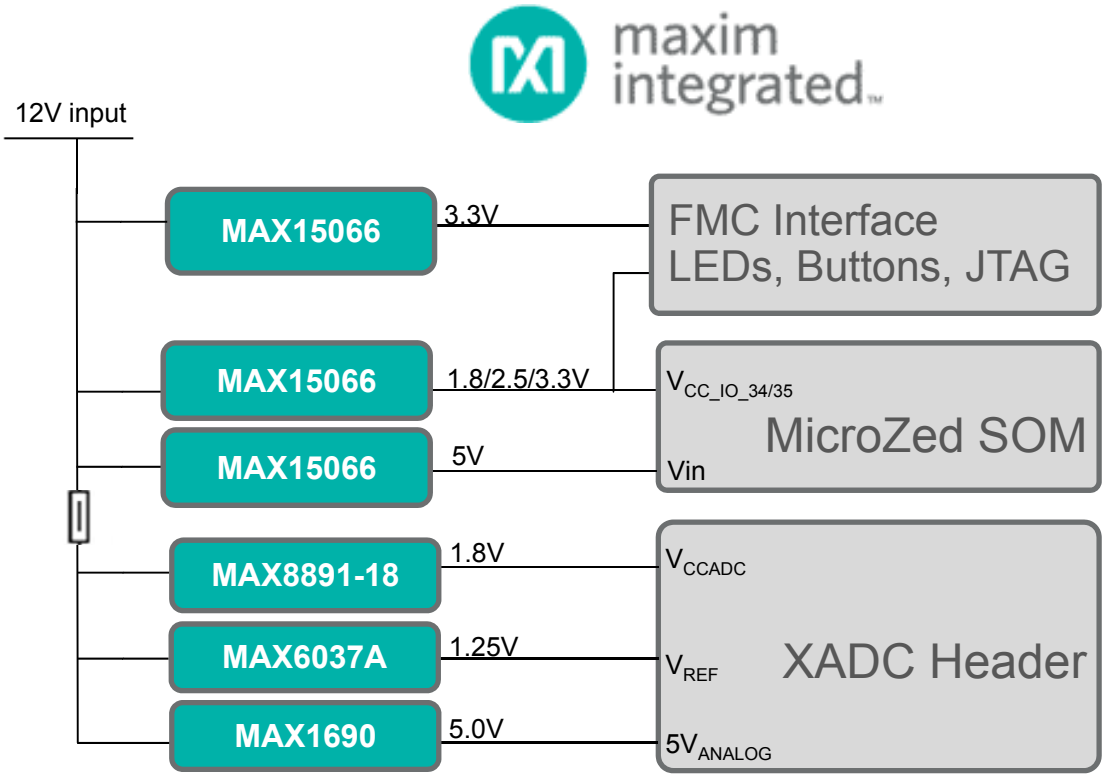
**MAX15066**
- Integrated MOSFETs
- 4.5 to 16V input
- 4A output
- Up to 96% efficient
- +/- 1% accuracy

**MAX8891-18**
- 150mA High PSRR LDO

**MAX6037A**
- +/- 0.2% reference

**MAX16190**
- Low Iq, high voltage LDO

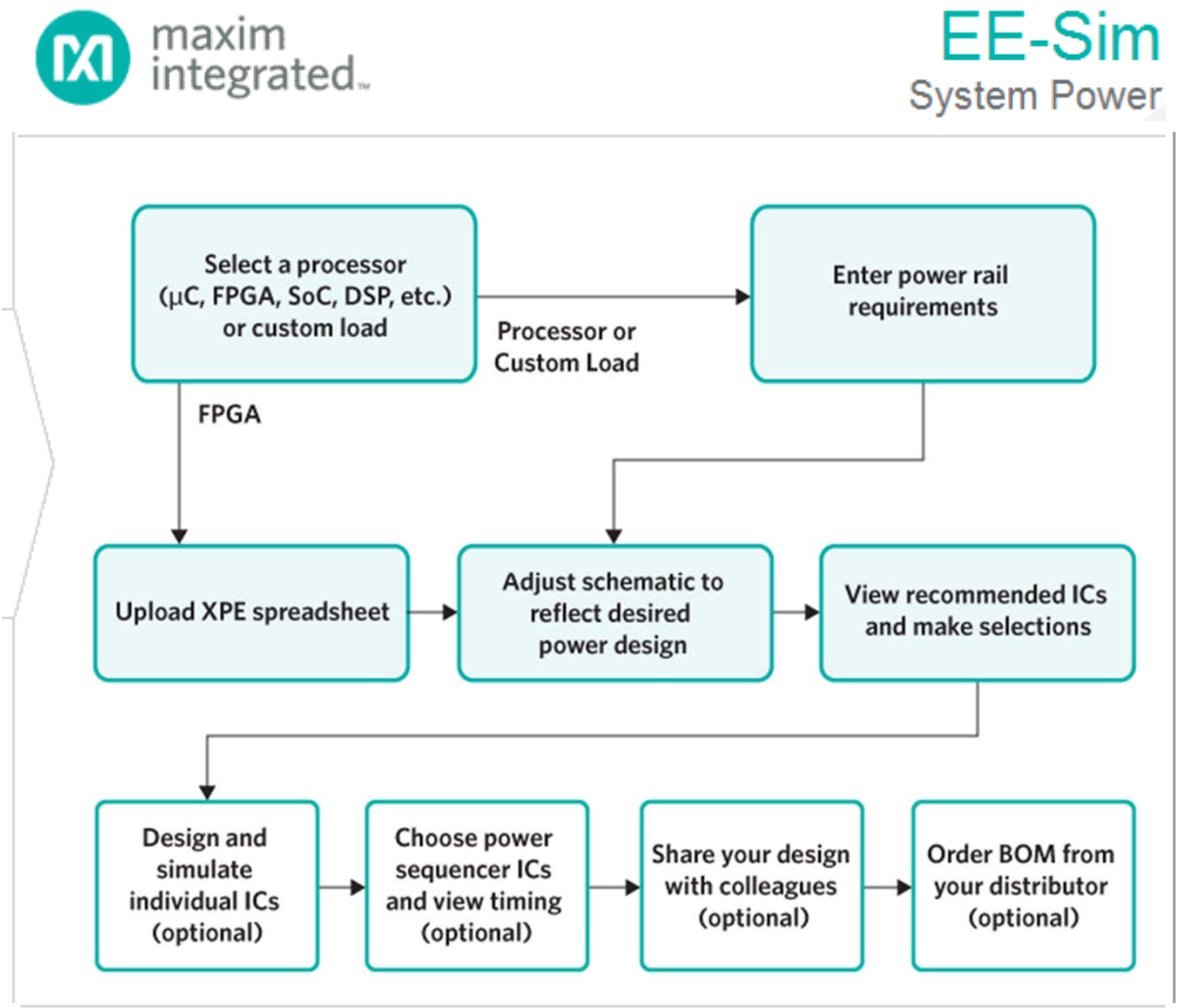
**MAX17501 (I/O Carrier)**
- Integrated MOSFETs
- 4.5V to 60V input
- 500mA output
- +/- 1.7% accuracy



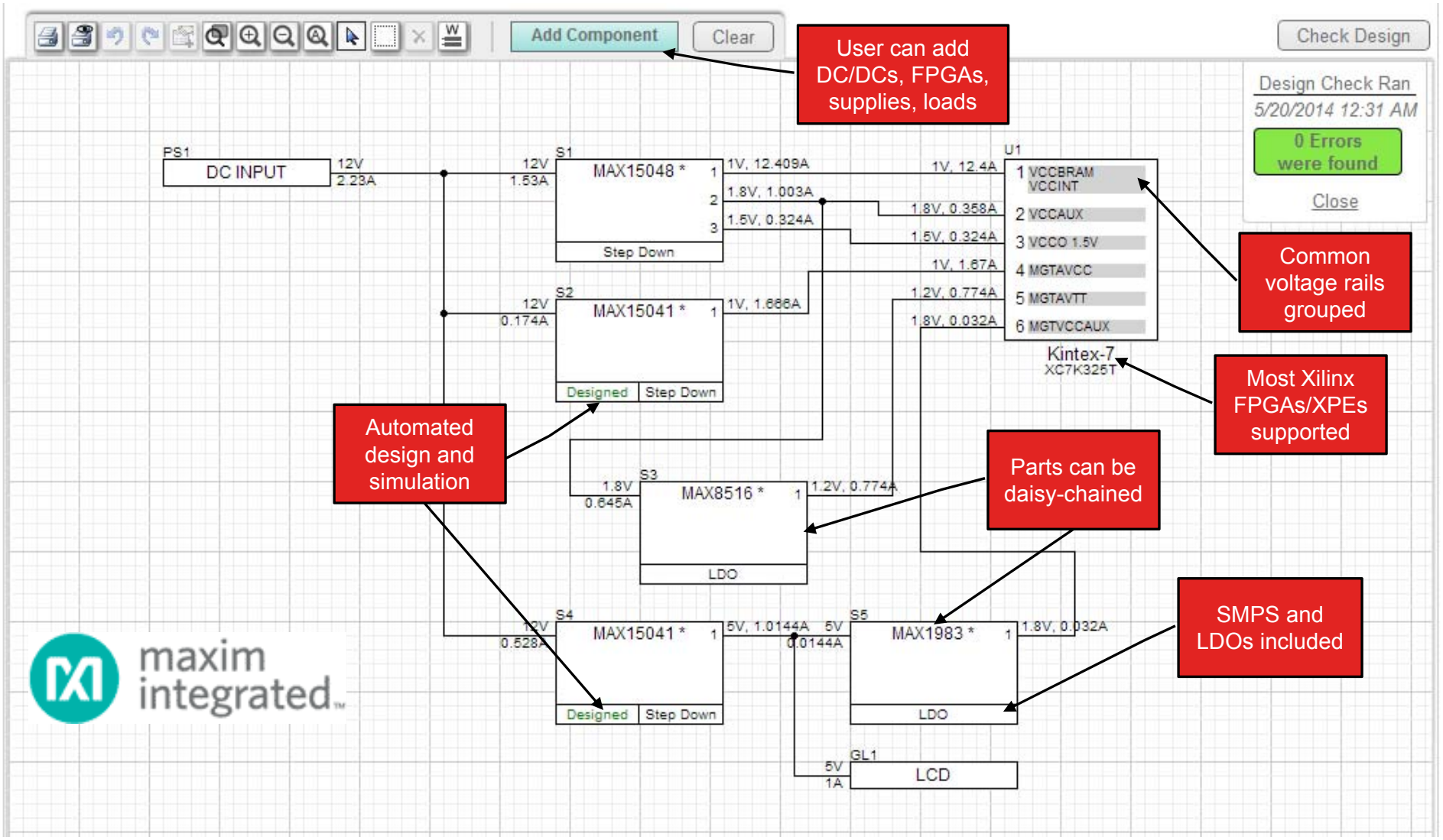

**I/O carrier (12 PMOD interfaces, no FMC interface)**
- 5V input
- MAX17501 for 3.3V supply
- Two MAX15066 devices supporting independent adjustable outputs for both $V_{CC\_IO\_34}$ and $V_{CC\_IO\_35}$

# EESim Design Tool

- Greatly speeds multi-rail, multi-load power designs
- Import your XPE spreadsheet
- Recommends ICs from over 500 parts, validates your choice
- Design and simulate switcher in minutes (modeled ICs)
- Sequencing tool
- Complete documentation PDF
- Design sharing

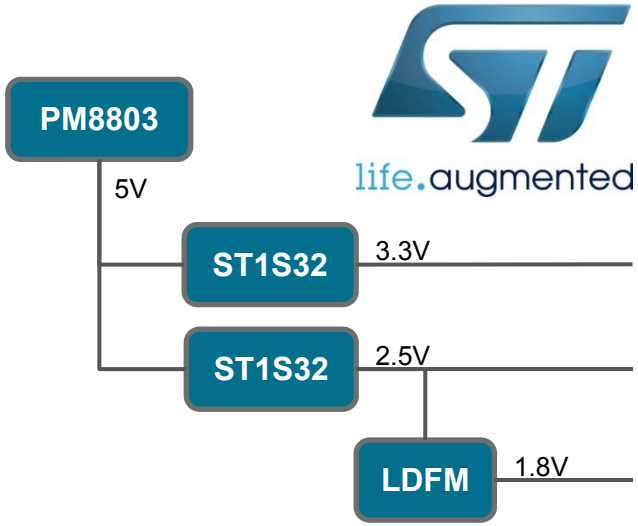


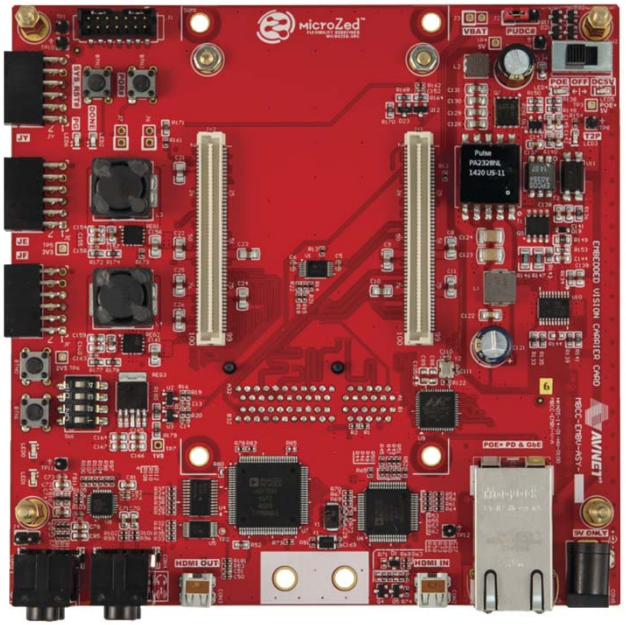
# EESim Design Tool Example



# Network Embedded Vision Design

- Embedded Vision Carrier Card
  - PM8803 PoE+ controller
    - Provides up to 25.5W (PoE+)
    - Fully supports 802.3at standard
  - ST1S32 synchronous regulators
    - 2.8V – 5.5V input
    - 4A output
    - 1.5MHz
    - Compact 4x4mm package
    - high efficiency
  - LDFM 500mA LDO
    - 300mV max dropout at full load
    - 2.5V – 16V input
    - Enable and PGOOD

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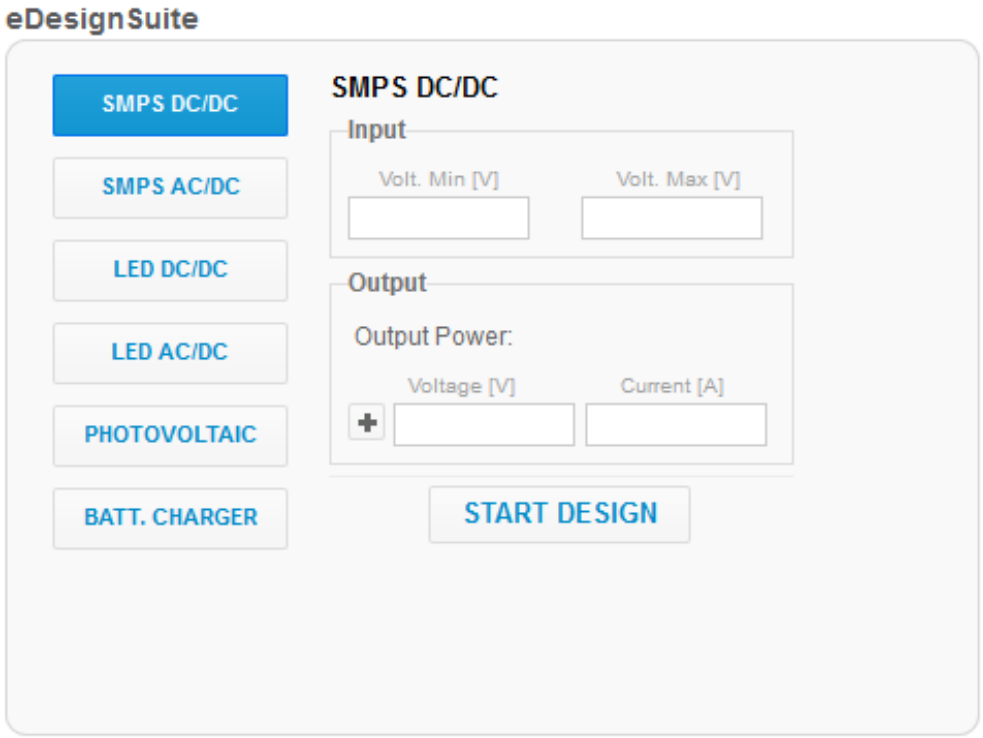
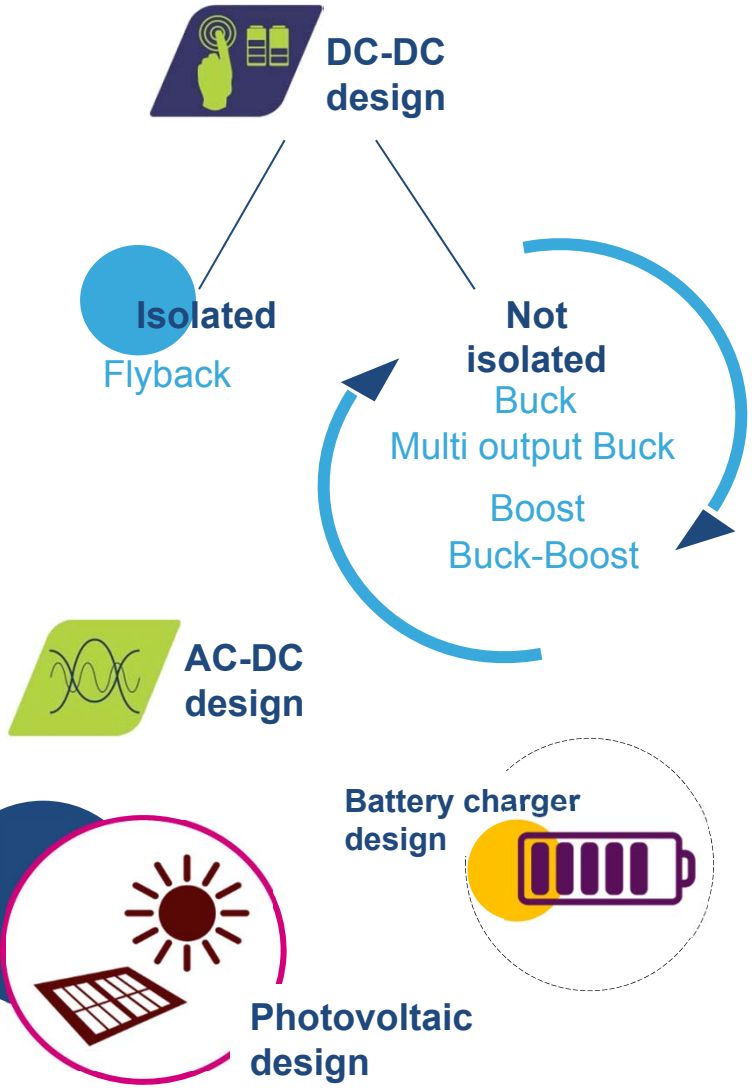
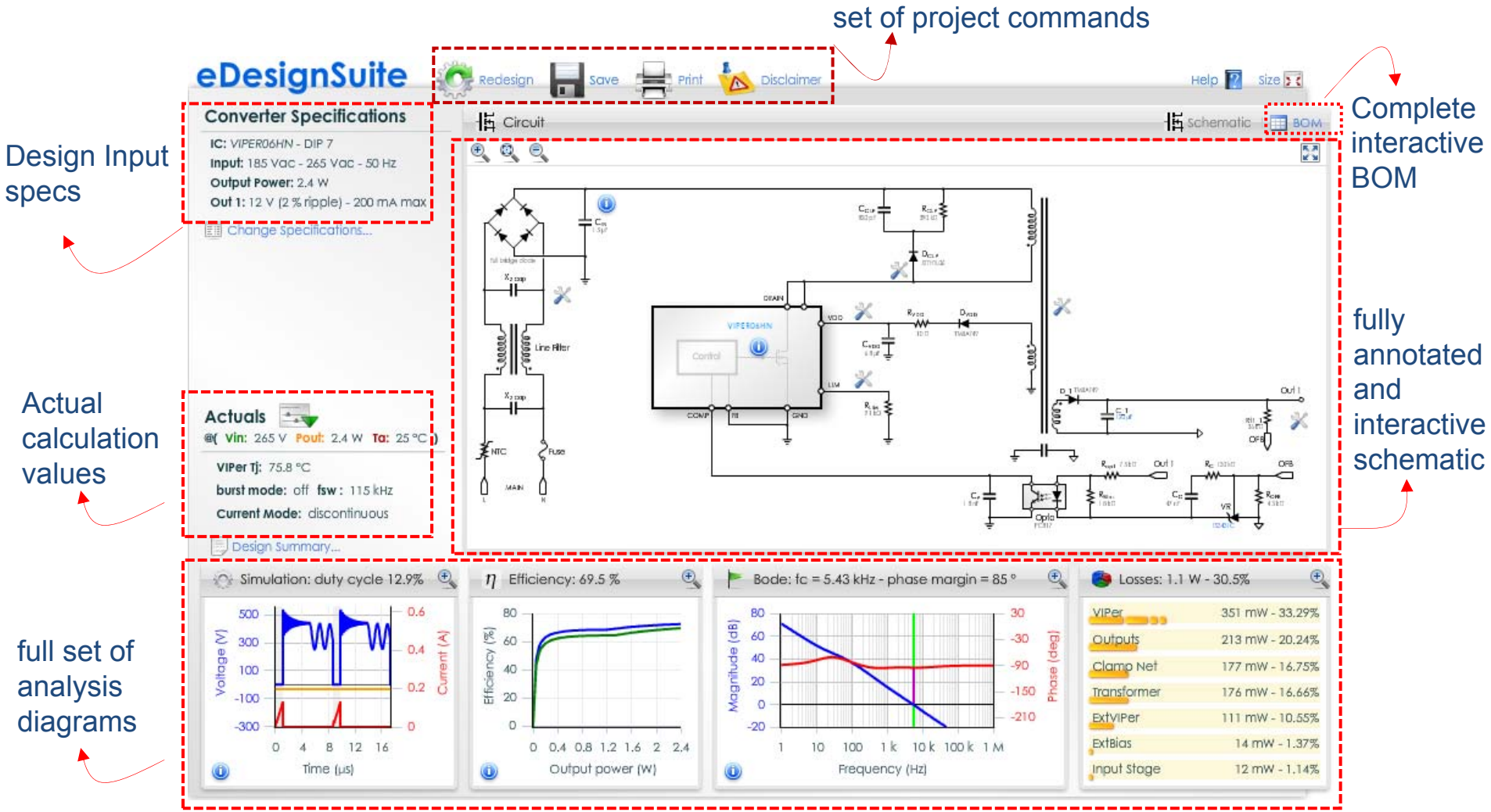
# STMicroelectronics DesignSuite



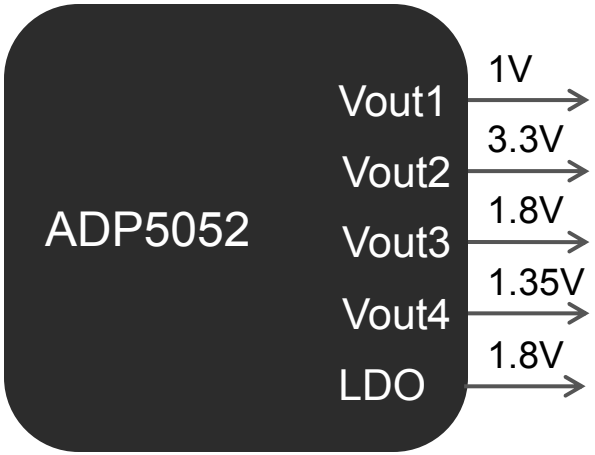

www.st.com/edesignsuite

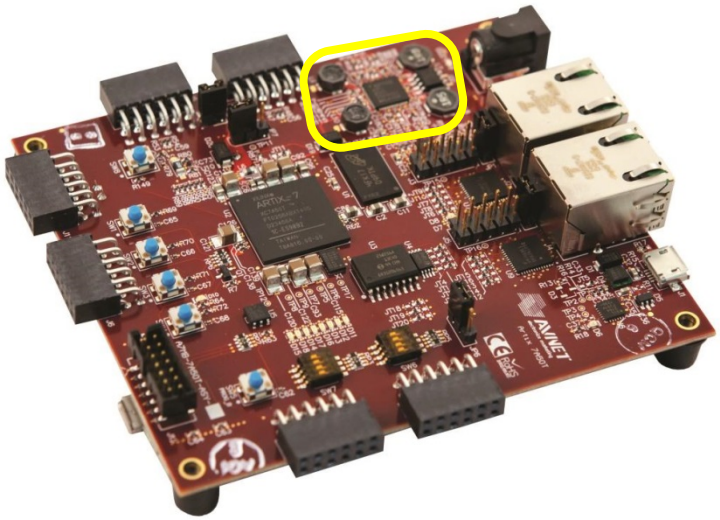
# eDesignSuite



# Artix 7 Reference Design Example

- Artix 7A50T
  - ADP5052
    - Highly integrated Power Management IC
    - 4x switching outputs plus a single LDO
    - Complete power solution in a single device
  - Several devices in the ADP505x family with slightly different features



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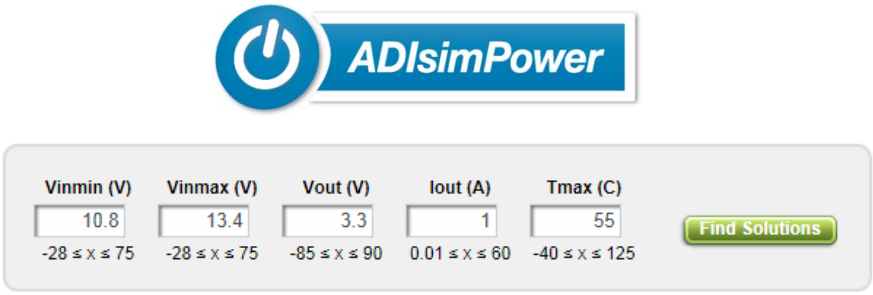
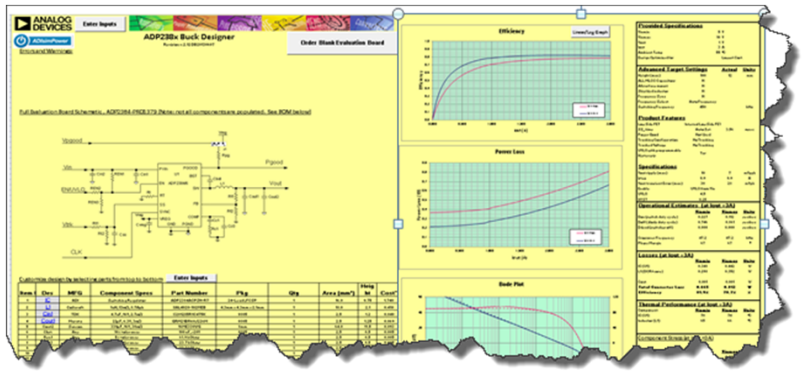
# ADIsimPower Design Center

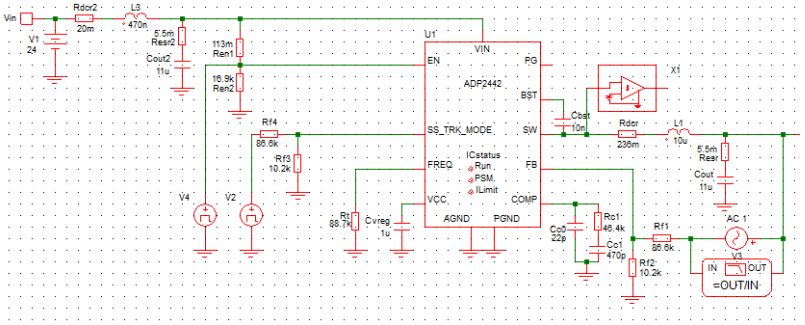
STEP #1:
**SELECT: ADIsimPOWER Selector**
www.analog.com/ADIsimPower
Smart selector
Identify the best part and topology
300 parts covered
10 different topologies




STEP #2:
**DESIGN & OPTIMIZE: ADIsimPOWER Designer**
Full design capability in minutes
No need to read the datasheet
Real Components behavior
Full Schematics, BOM and Performance data



STEP #3:
**SIMULATION: ADIsimPE**
ADIsimPE (Personal Edition) SIMetrix/SIMPLIS
Application schematics and component library
Integration with Power design tools



# Call to Action

- Follow design guide documents for ensuring a proper power system design
  - PCB design guides (7 series UG483, UltraScale UG583)
  - Transceiver design guides (7 series UG476, UltraScale UG576)
- Proper power budgeting should be done before every design
  - Utilize XPE design tool www.xilinx.com/power
  - Budget for the entire system up front and consider power during layout
- Consider thermal management requirements
  - Make sure heatsinks and fans are used when necessary
- Download this presentation at www.xfest2014.com
  - Available September 15th Q&A forums for each course
- Reference designs and design tools are available from Avnet and several of our manufacturers
  - Visit www.em.avnet.com/xilinxpowerdesigns
  - Visit www.em.avnet.com/powerdesigntools
  - Visit design booths and demo area


Thank You
Asante
Shukria
Dhanyavadagalu
Vinaka
köszönöm
Kiitos
Maake
Manana
Dankon
Kam Sah Hammida
Matondo
Terima Kasih
Taiku
Tack
Dank Je
Dankscheen
спасибо
Mauruuru
Biyan
Blagodaram
Ngiyabonga
Dziekuje
Chokrane
Diolch i Chi
Grazie
Juspaxar
Arigato
Mochchakkeram
Gracias
Khap
Tingki
Paldies
நன்றி
धन्यवाद
cảm ơn bạn
Gratias Tibi
Ua Tsaug Rau Koj
Bedankt
Dakujem
Grazas
Kia Ora
Kop Khun
Obrigado
Děkuji
Nirringrazzjak
Di Ou Mèsi
ありがとう
Suksama
Hvala
Nuwun
Rahmat
Welalin
Djiere Dieuf
Matur
谢
谢
Misaotra
Danke
Merci
Go Raibh Maith Agat
Eskerrik Asko
Salamat
ขอขอบคุณคุณ
Najis Tuke
хвала