High Speed Signal Processing in UltraScale

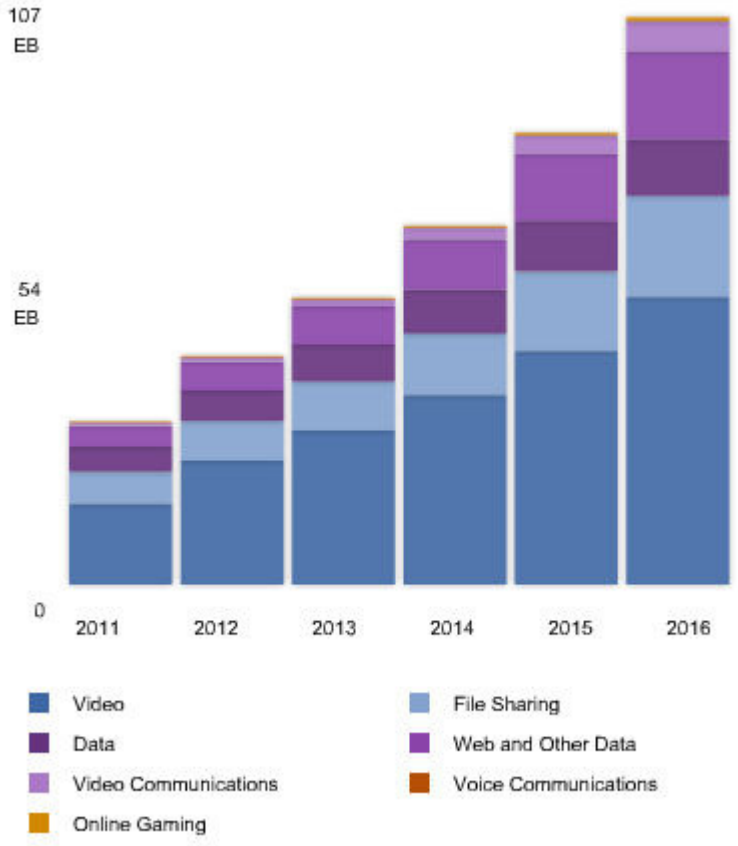
With Wideband Data Acquisition using JESD204B

Accelerating Your Success™

The Insatiable Demand for Bandwidth

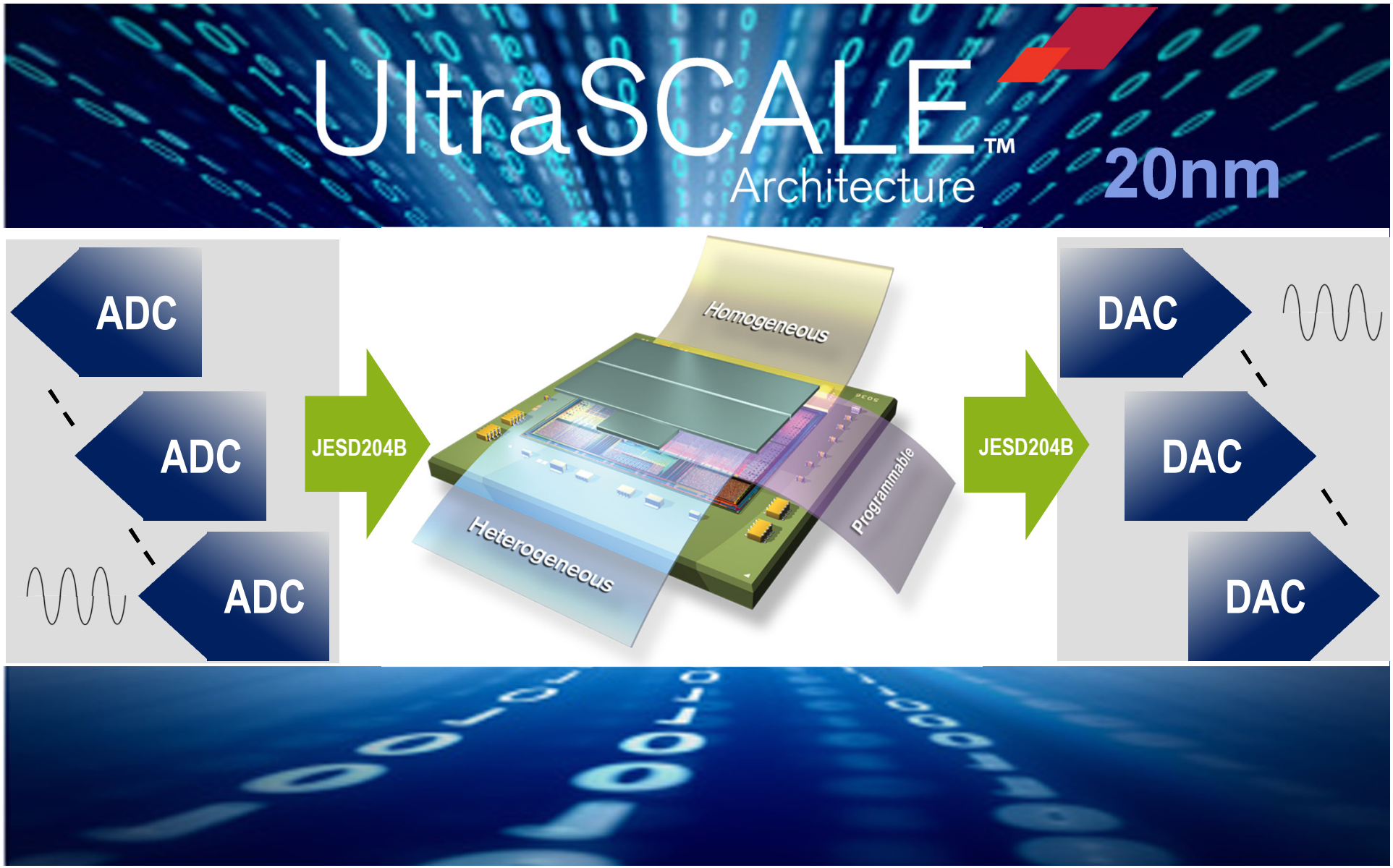
- In 2016, global IP traffic will reach 107.3 Exabytes per month
- Global IP traffic has increased eightfold over the past 5 years, and will increase threefold over the next 5 years
- The number of devices connected to IP networks will be nearly three times as high as the global population in 2016
- Traffic from wireless devices will exceed traffic from wired devices by 2014

107 Exabytes of IP Traffic per Month by 2016



*Cisco VNI May 2012

Xilinx UltraScale Massive Bandwidth and Processing



Course Objectives

- Explore Xilinx UltraScale architecture for digital signal processing and multi-gigabit serial transceiver connectivity
- Preview latest-generation wideband analog data converters with JESD204B high-speed serial interface technology
- Investigate parallel digital signal processing techniques for FPGA-based wideband data acquisition systems

Agenda

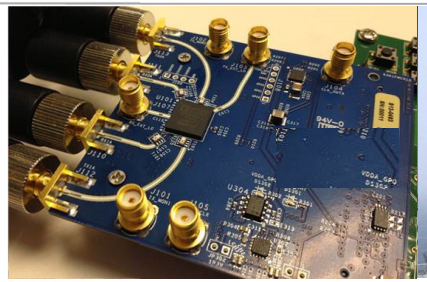
- Xilinx UltraScale features for wideband data acquisition
- JESD204B data converter high-speed serial interface
- Xilinx JESD204B IP
- JESD204B data acquisition on Kintex UltraScale
- Digital signal processing for wideband data acquisition

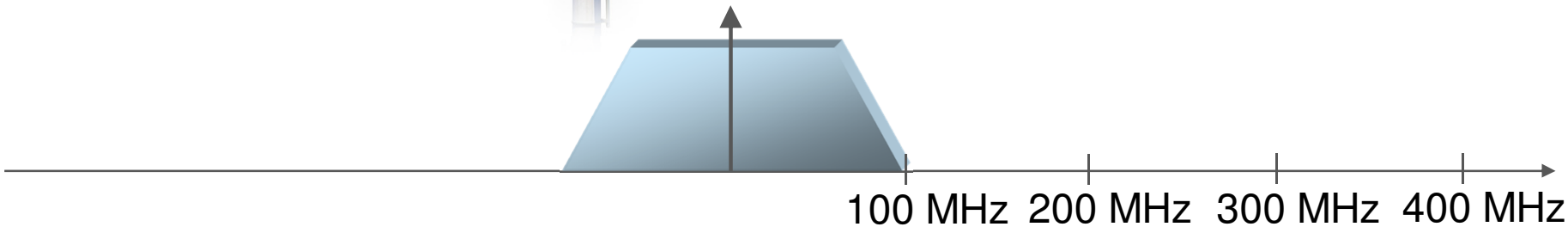
Xilinx UltraScale Architecture Overview

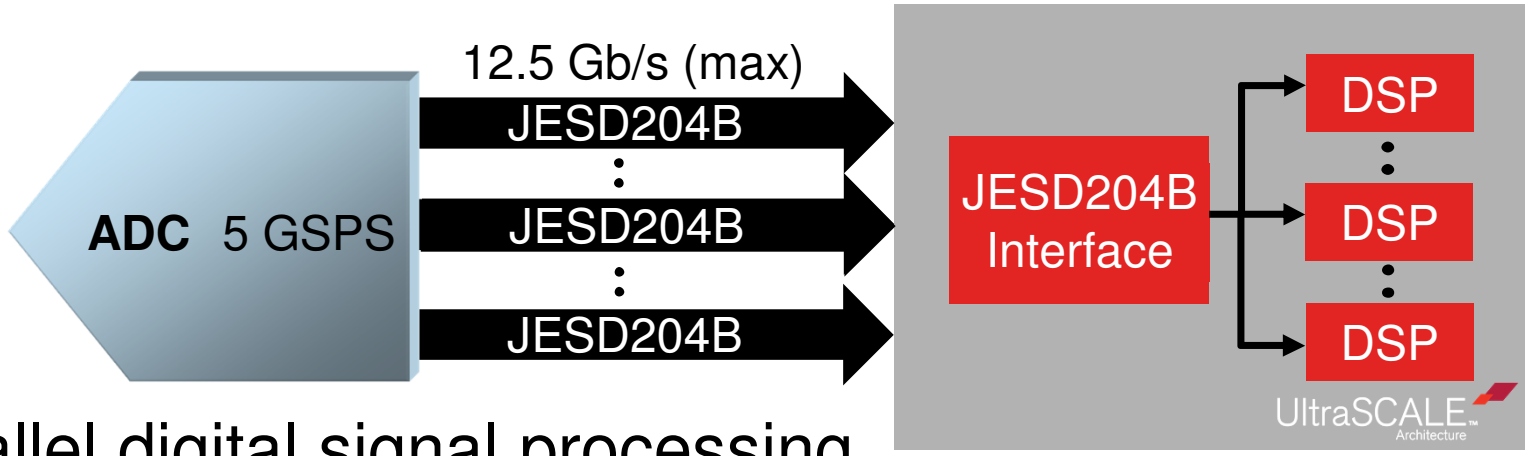
With Emphasis on DSP and Serial Transceivers

The Quest for Bandwidth







- Parallel digital signal processing
- JESD204B high-speed serial interface

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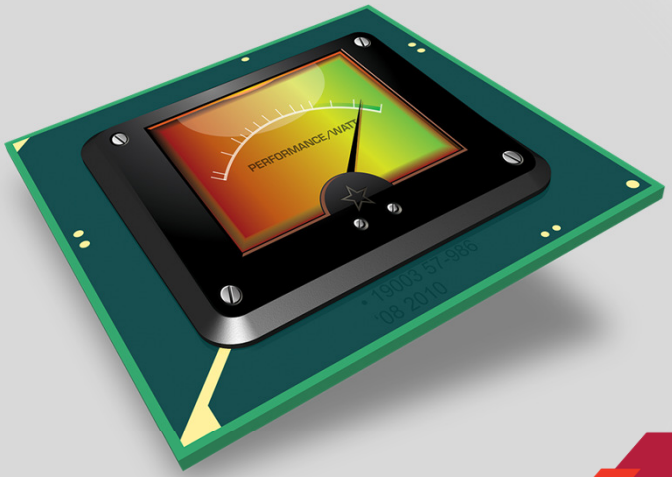
UltraScale Innovations

VIVADO™
Co-Optimized

Security
AES-GCM mode,
greater key protection,
more authentication schemes



Transceivers
12.5G low speed grade
16G & 28G backplane
33G chip-to-chip

27x18

DSP
Wider multipliers,
fewer blocks per function

SLR0 SLR1

SSI Technology
Virtual monolithic die

DDR4

Memory I/O
40% higher data rates
20% lower power

UltraSCALE™
Architecture

Integrated IP
JESD204B
100G Ethernet MAC
150G Interlaken

Block RAM

Block RAM
Hardened data cascading
Improved power, performance

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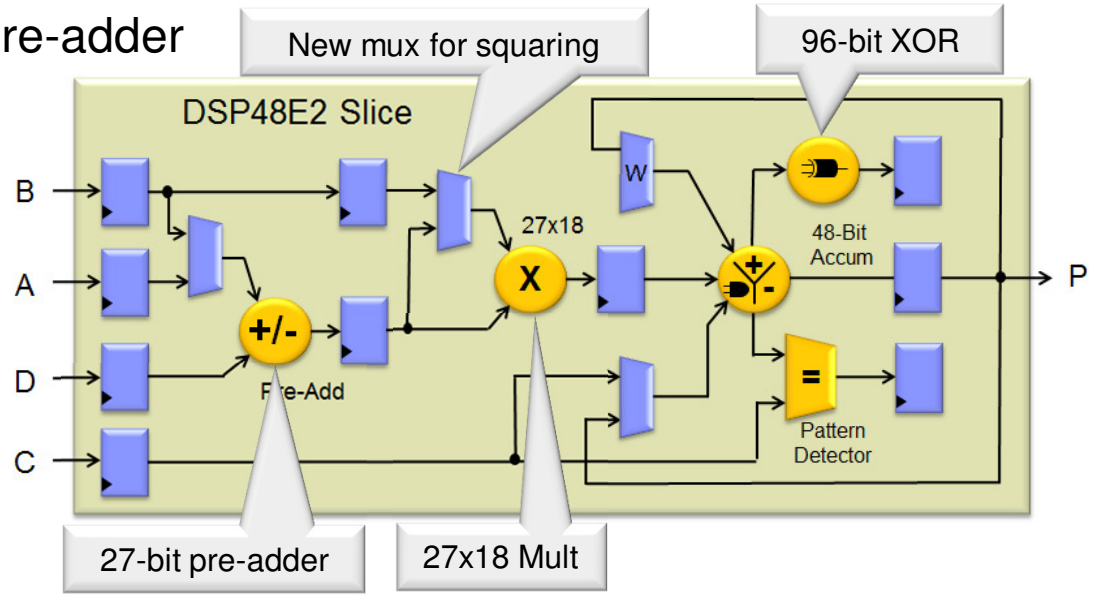
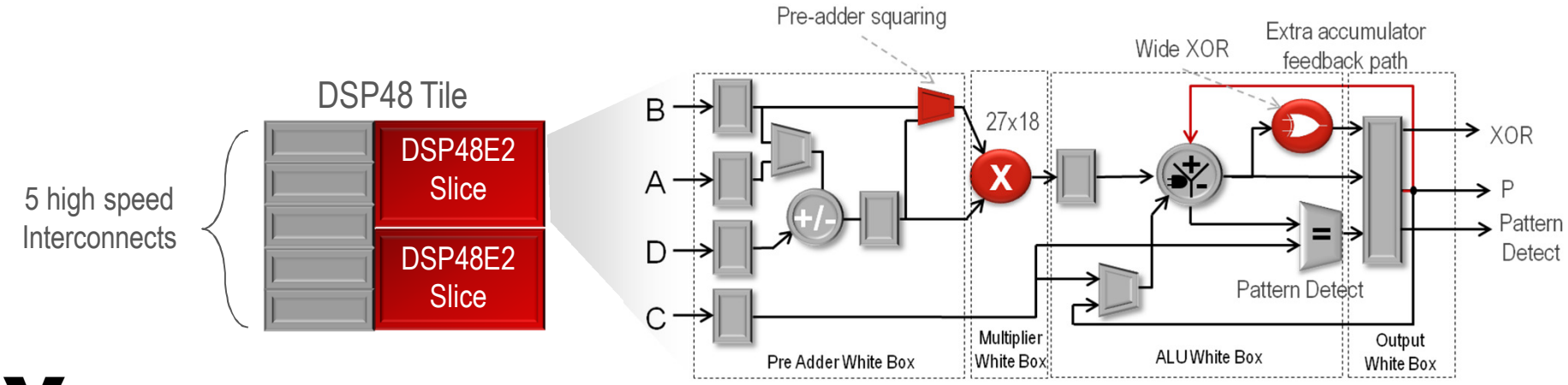
UltraScale DSP Slice Features

- UltraScale DSP slice is a superset of 7 Series DSP48E2
  - 27x18 multiplier and 27-bit pre-adder
  - 96-bit MACC
  - SIMD support
  - 48-bit ALU
  - Pattern detect
  - 17-bit shifter
  - Dynamic operation (cycle by cycle)
  - Squaring: $(A+/-D)^2$, Wide XOR (up to 96 bit) and WMUX product feedback
  - 8,000 GMAC/s



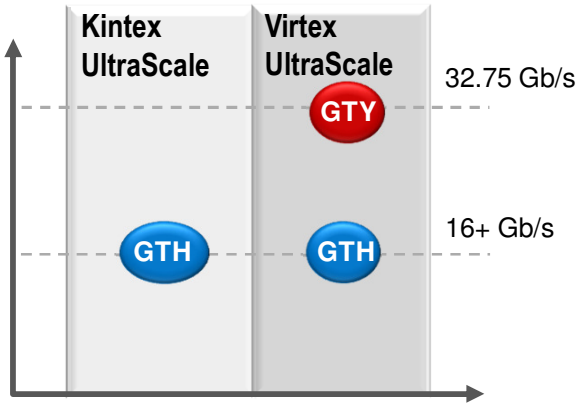
Enhanced DSP Sub-Systems in UltraScale

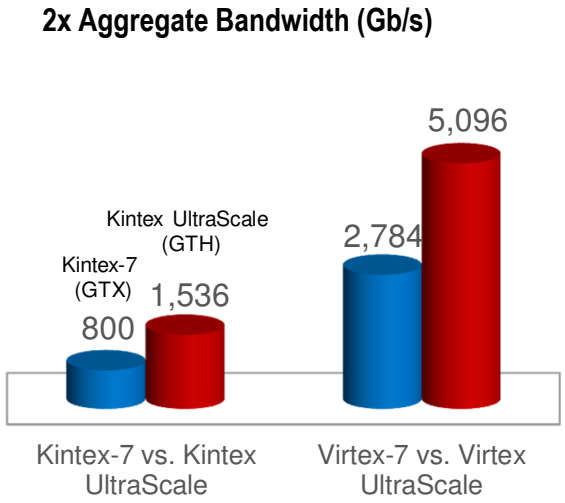
Feature	Benefit
27x18 multiplier in a DSP slice; 35x28 support in a DSP tile (2 slices)	• Optimal performance per block • Implement double-precision floating point in two-thirds the fabric
Pre-adder squaring	• More efficient motion estimation in video applications • Perform “sum-of-square-difference” calculations in 50% fewer resources
Extra accumulator feedback path	Implement complex multiply-accumulate in half the resources
Wide XOR	Implement EFEC, CRC, ECC functionality
White box modeling	Full visibility with accurate simulation and debug

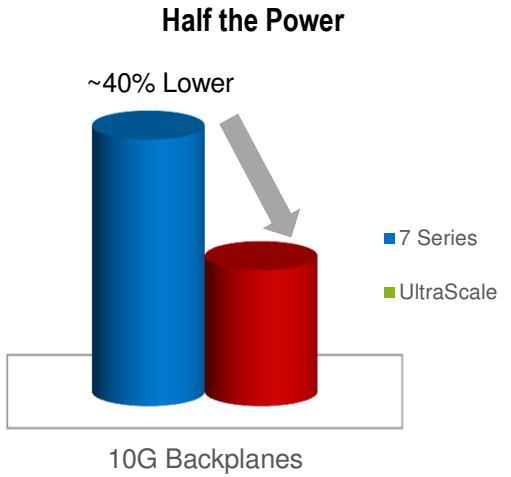


Delivering Massive I/O Serial Bandwidth

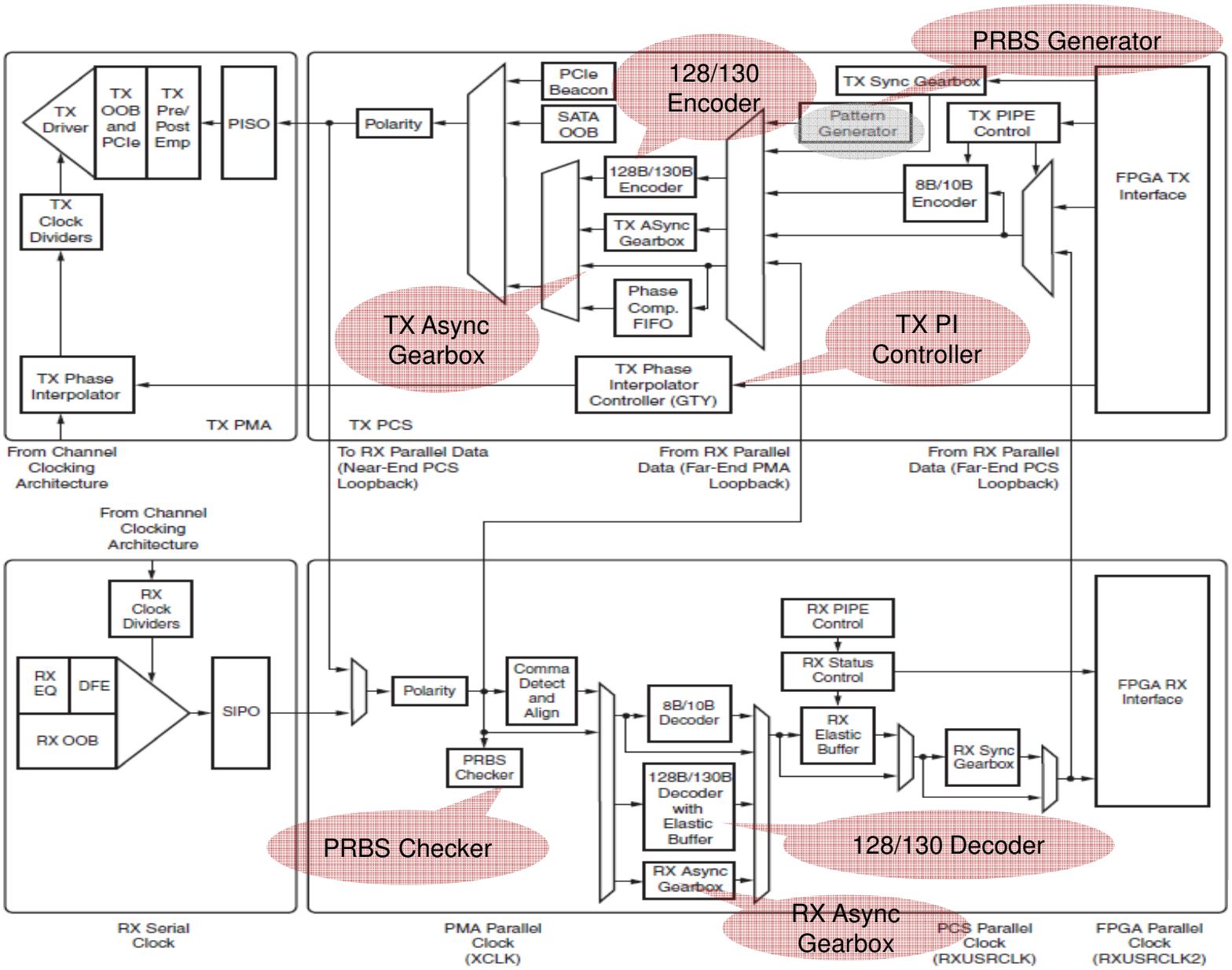
Feature	Benefit
GTH (16 Gb/s) for price-performance	• 12.5Gb/s performance in the lowest speed grade, across all temperature ranges • Enabled std: PCIe Gen4 (16G), JESD204B (12.5G), CPRI (16.3G), Serial Memory (HMC & MoSys)
GTY (32 Gb/s) for highest performance	• 28Gb/s (CEI-25G-LR) backplane support for Nx100G to 400G systems • Support for Interlaken, OTU4 over CFP4, 802.3bj (28G Ethernet backplane)
Major power reduction	~40% lower power for 10G backplanes
Continuous auto-adaptive equalization	Continuously optimizes link margin over PVT in increasingly challenging channel conditions





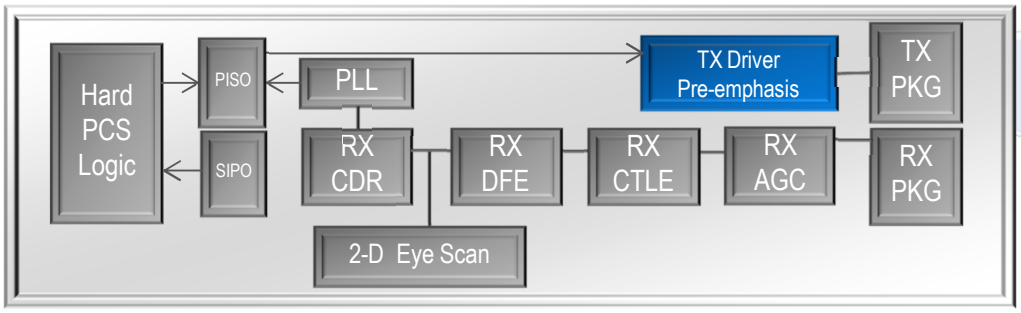


UltraScale Transceivers Channel Block Diagram

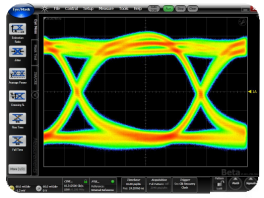


Auto-Adaptive Receiver Equalization in Action

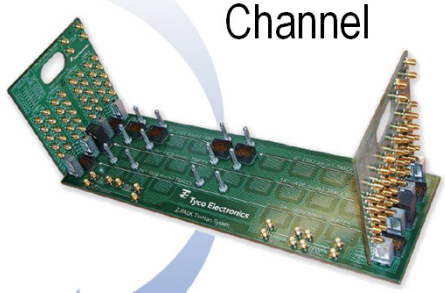
Transceiver Architecture



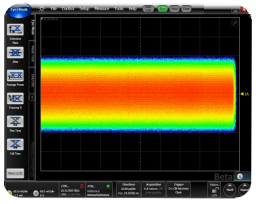
Open Eye at Transmitter

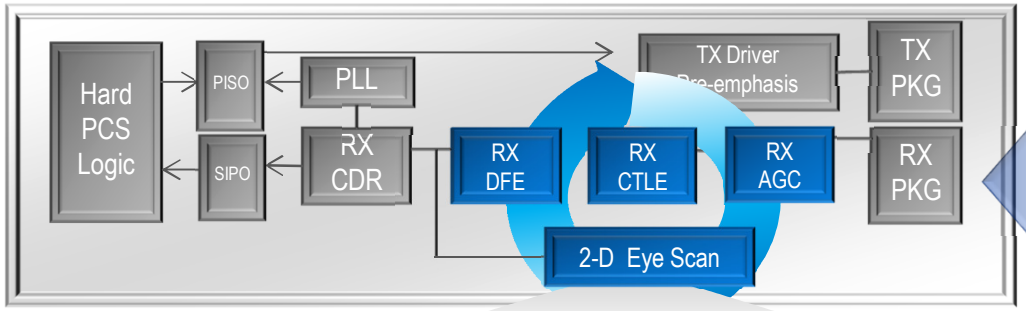


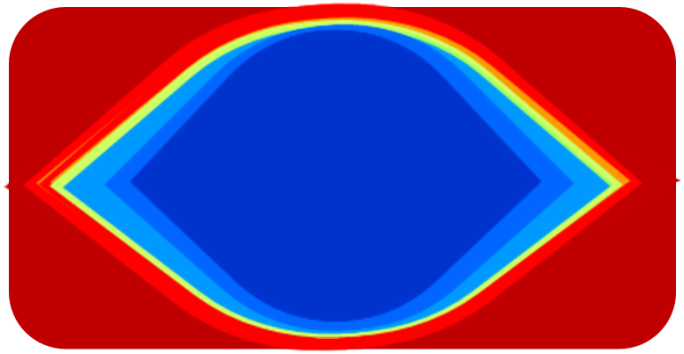
Lossy Channel



Closed Eye at Receiver







Open Eye Post-Equalization

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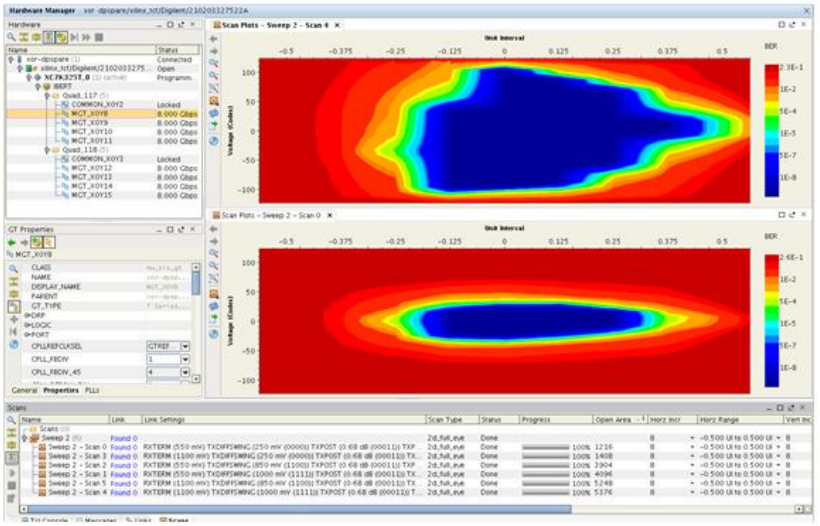
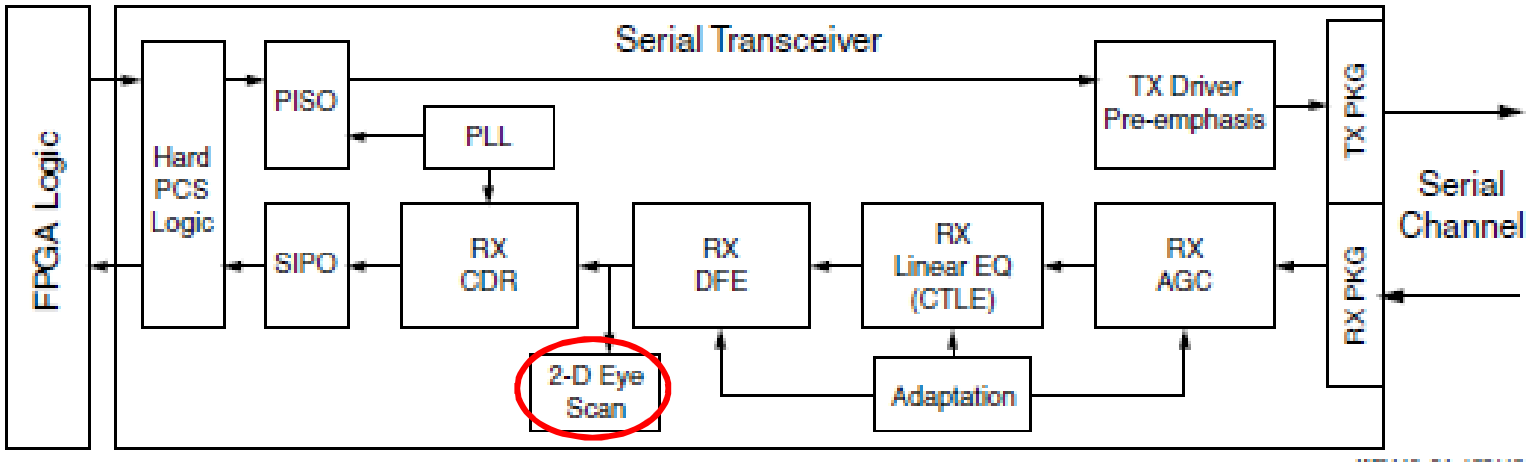
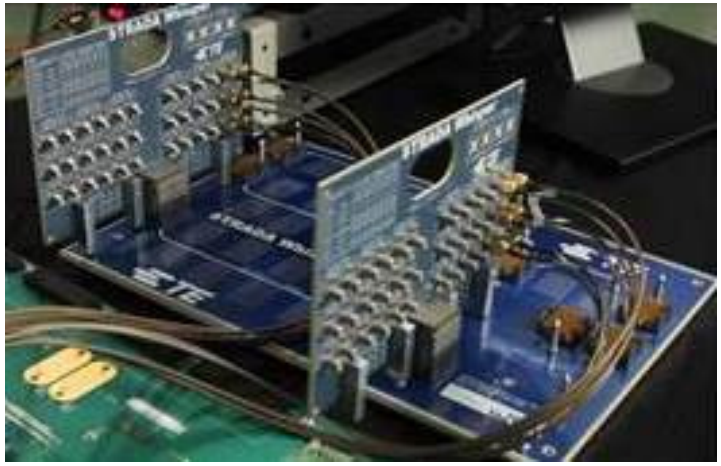
2D Eye Scan – Verify JESD204B Connectivity

- Dedicated circuitry within UltraScale GTH transceiver
  - On-chip scope to visualize signal quality
  - Non invasive, no impact on your signal
  - Accelerates debugging
- Scans the eye to show signal integrity
  - Reports Bit Error Rate
  - Vivado Serial IO Analyser GUI Tool



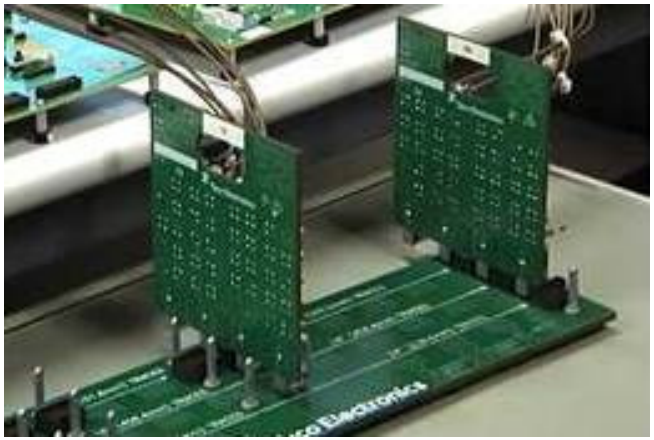


Kintex Ultrascale GTH- 16.3 Gb/s over Backplane



- TE STRADA Whisper
  - Newest materials allow for longest traces at highest rates
    - (Megtron-6)
  - 30in of backplane + linecards, cables and board trace

- TE Z-PACK TinMan
  - 10G legacy backplane
  - 8in of backplane, 2x5in of linecard, cables and board trace
  - 26dB of total loss @ 8GHz
  - Large internal eye, lots of margin, headroom for additional length



Visit TE to identify best connector option for your system!

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TE connectivity Authorized Distributor

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STRADA Whisper Advantages

- Only proven 25Gbps connector in the market
- 1.5mm Un-mate Electrical Performance
- Robust Signal Pins and Ground Shields
- Scalability up to 56Gbps
- Best in Class EMI Performance
- Industry Leading Crosstalk Performance
- Skew-less Design Without Cancellation Tricks
- Flexible Design Options to Support all Architectures

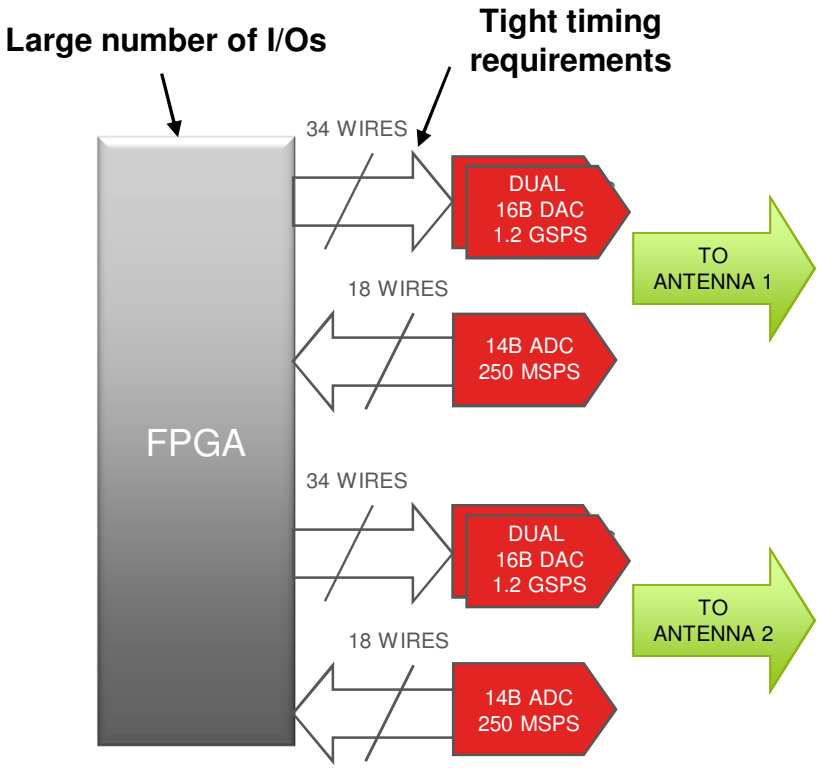
Visit TE to identify best connector options for your system!

JESD204B

Data Converter High-Speed Serial Interface

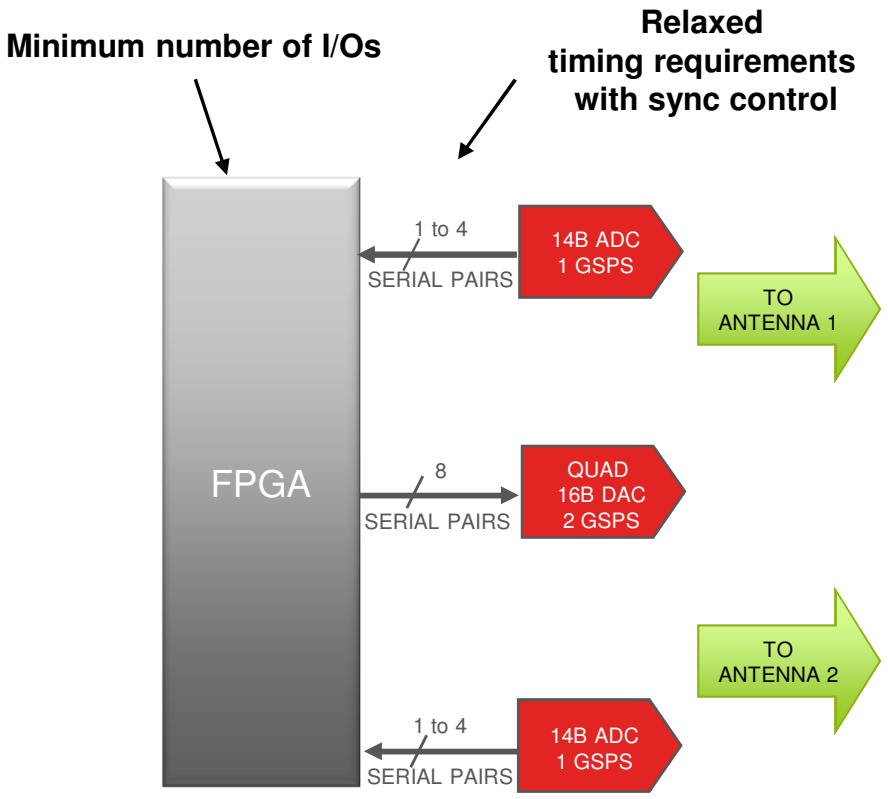
Why a new a Converter-to-FPGA interface?

Traditional data converter interface



- High pin count low speed parallel

High-speed serial interface

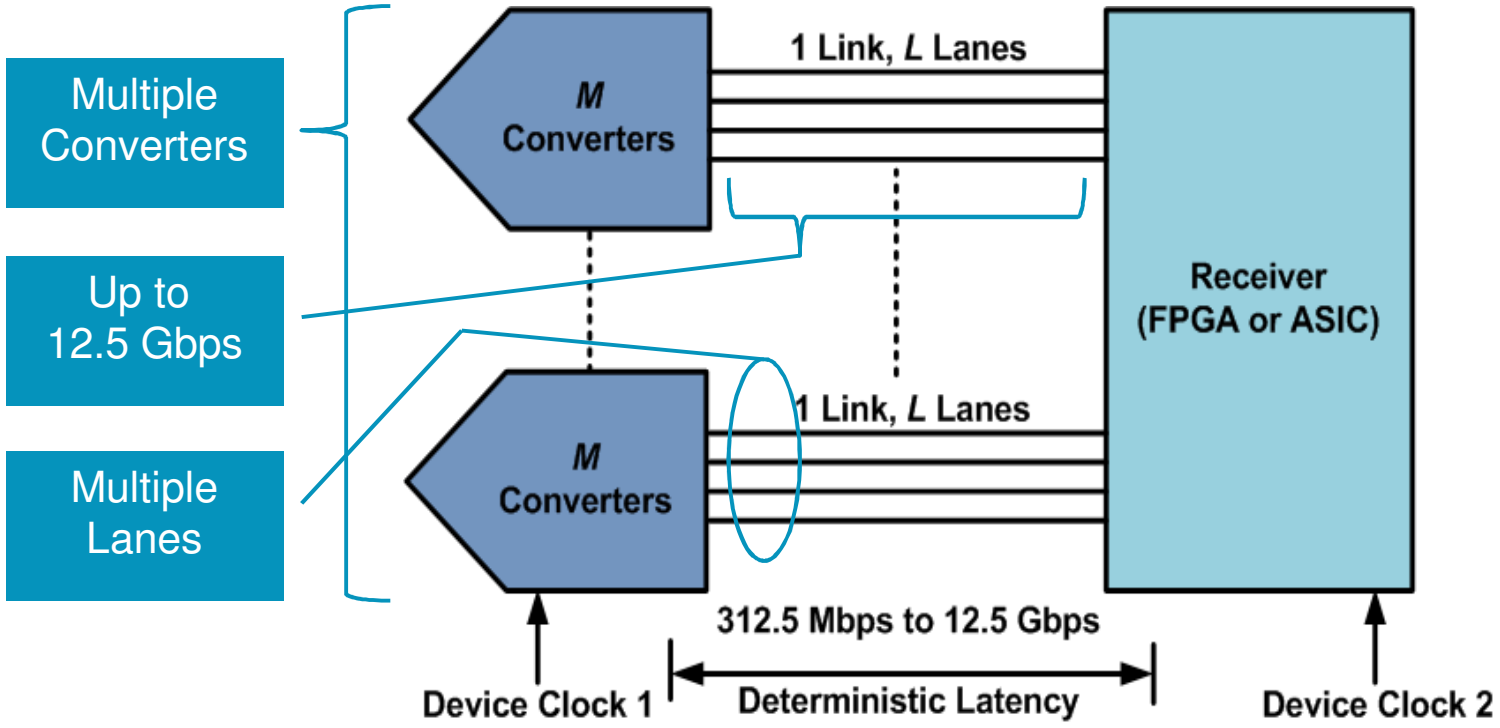


- Low pin count high speed serial

What is JESD204B?

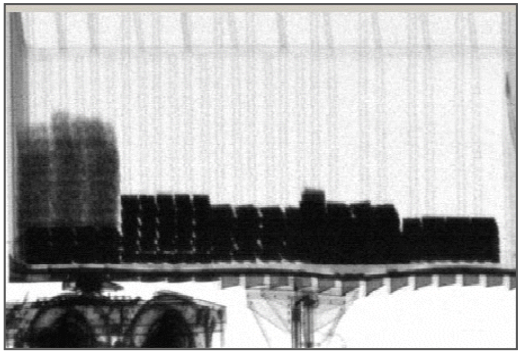
...

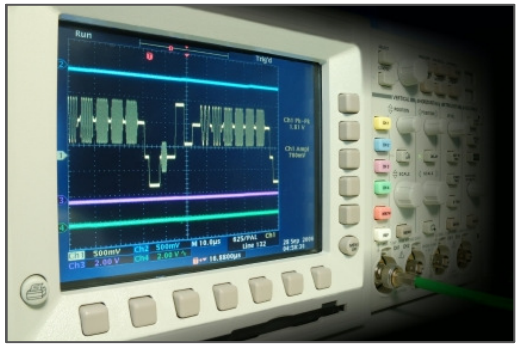
- Industry standard (JEDEC) defining multi-gigabit serial data link between data converters and a receiver (typically an FPGA or ASIC)



JESD204B Target Markets / Applications

- JESD204B solutions target high-end data converter and data acquisition applications
  - Wireless Infrastructure
  - Medical Imaging
  - Military Radar
  - Electronic Test & Measurement
  - CMTS* and Cable Access

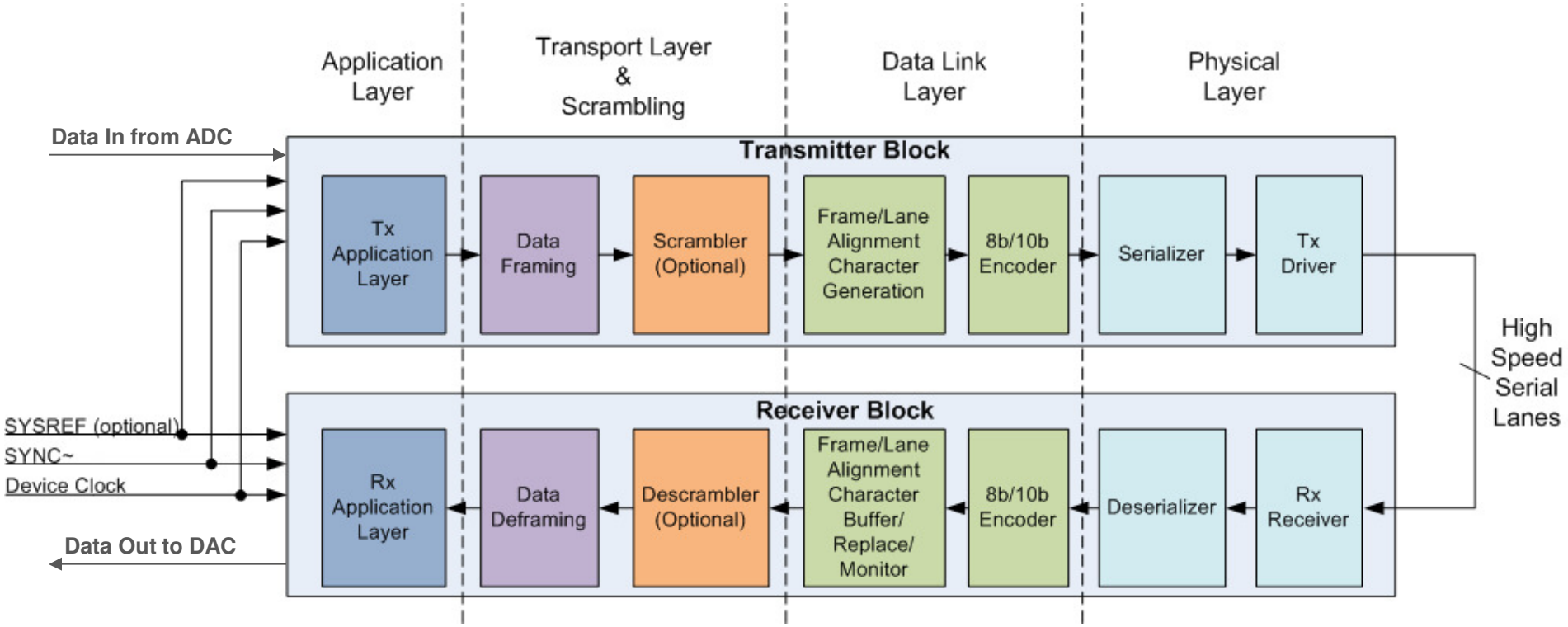




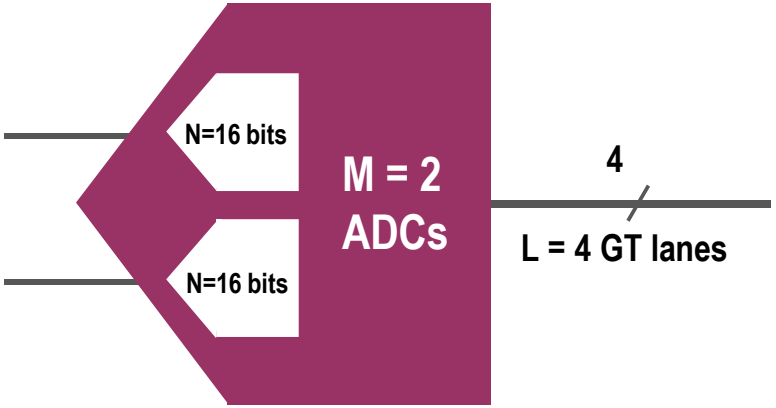
* Cable Modem Termination System

JESD204 Simplified System View

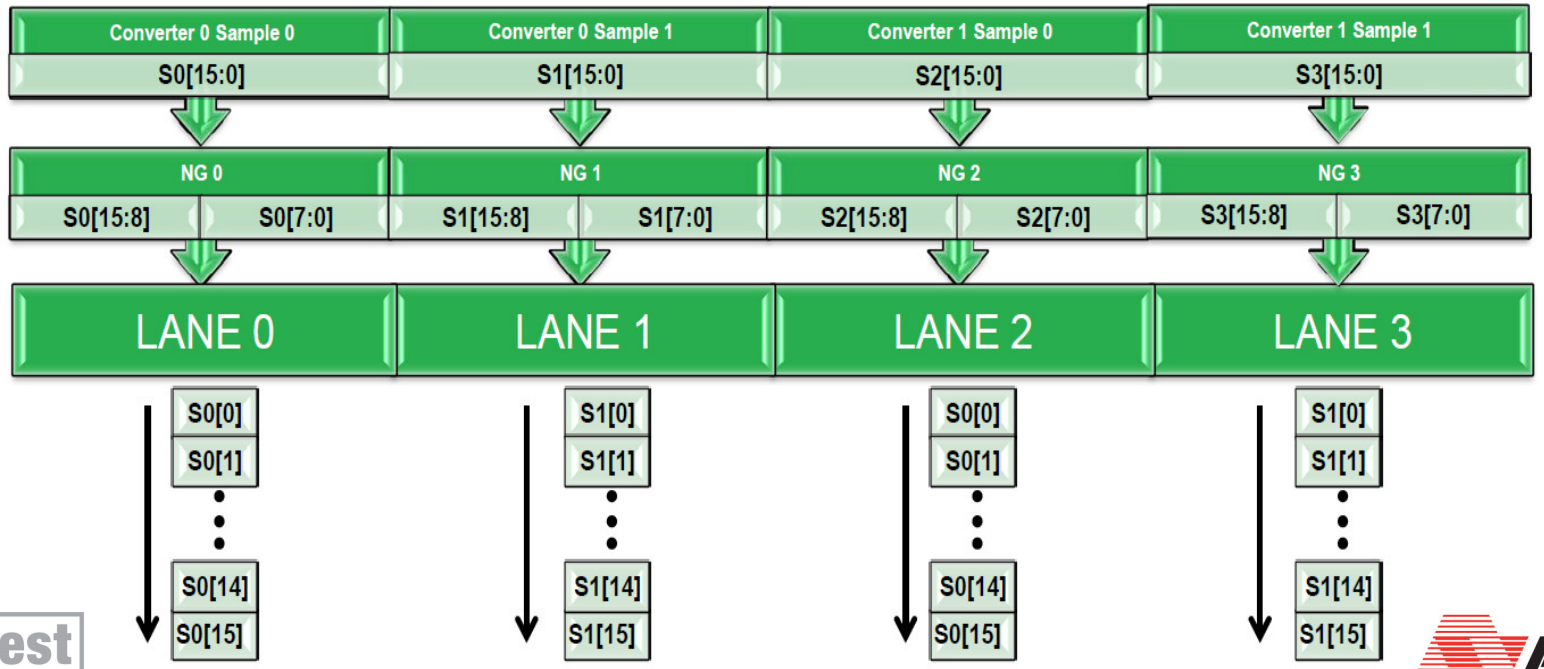
- Structured in layers similar to OSI model



JESD204B Transport Layer Mapping

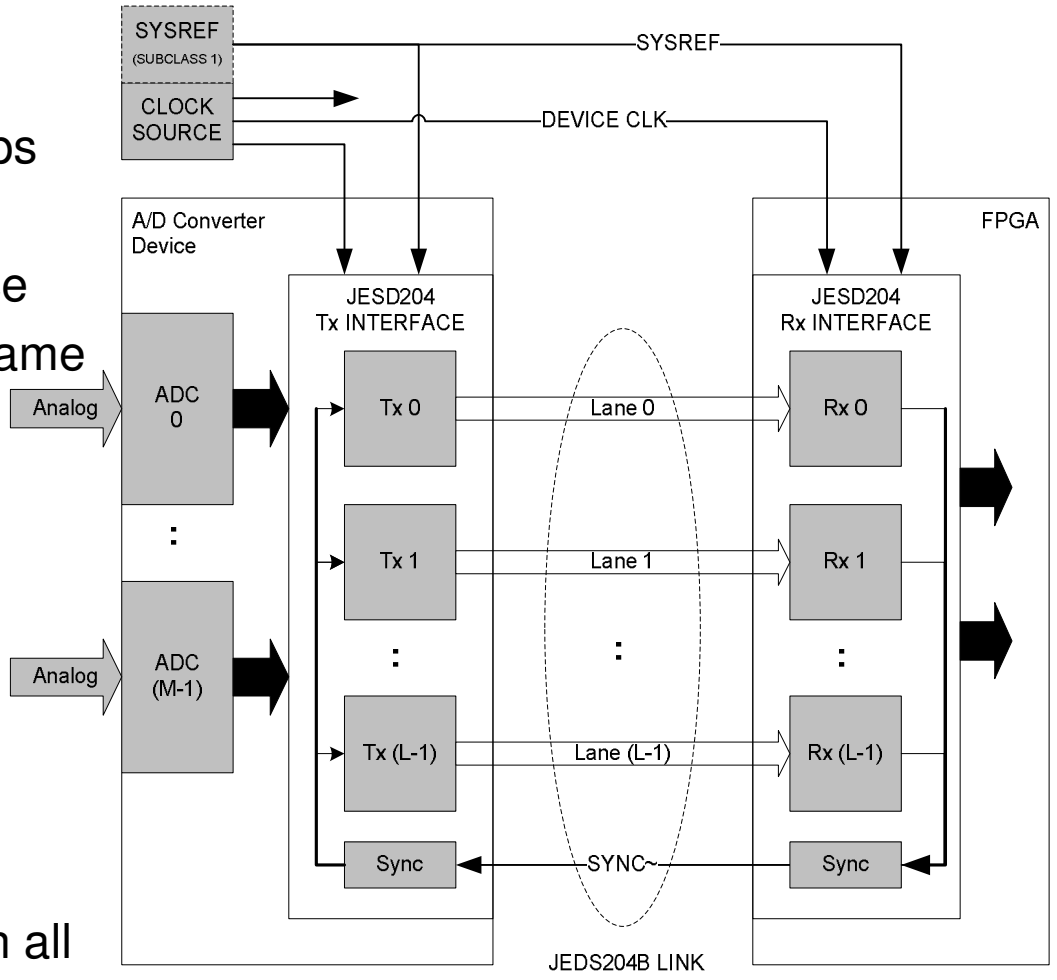


JESD204B Parameters		
L	4	GT Lanes
M	2	Number of converters
F	2	Octets / Frame / Lane
N	16	Sample word precision
N'	16	Nibble Group Size
CS	0	Control bits / Sample / Frame
S	2	Samples / Converter



JESD204B Physical Layer

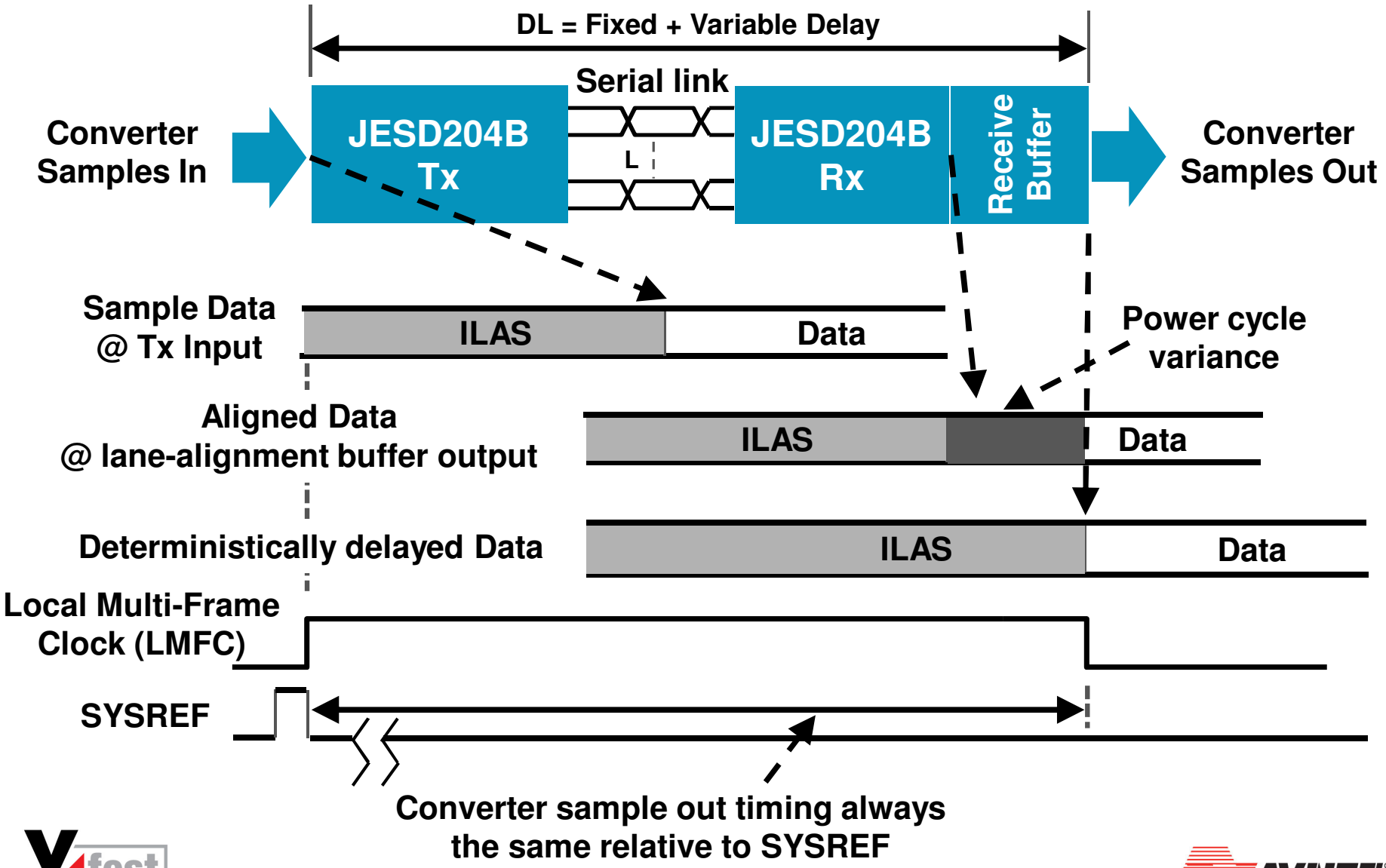
- L Serial Lanes (L = 1 to 32)
  - 8B/10B encoded (+ scrambling)
  - Line rates 312 Mbps to 12.5 Gbps
- Device Clock
  - Common master timing reference
  - Harmonic relationship to Multi-frame clocks
- SYNC~
  - RX to TX device, indicates RX synchronization
  - Rx can force resynchronization
- SYSREF (Subclass 1 only)
  - Distributed to all devices – synchronous to device clock(s)
  - Aligns Local MultiFrame Clock in all devices for deterministic latency



JESD204B - Subclasses

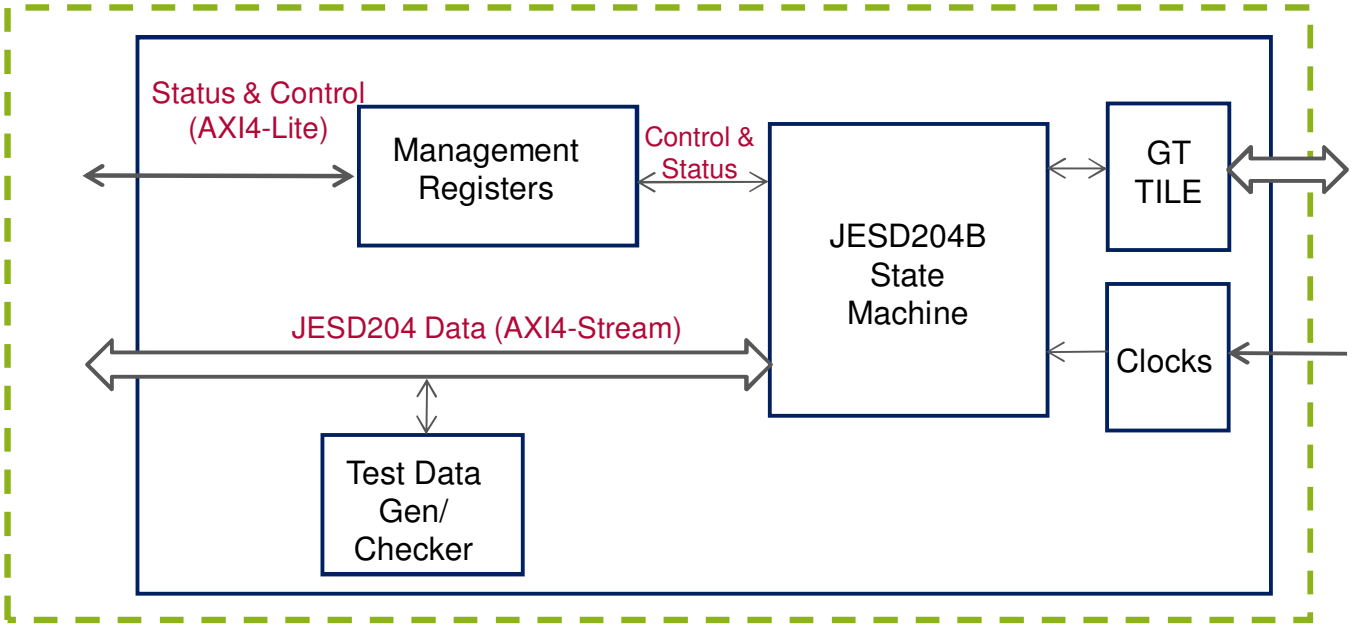
- Subclass 0
  - No deterministic latency support
  - Effectively JESD204A with higher line rates (up to 12.5G)
- Subclass 1
  - Uses additional discrete signal SYSREF for deterministic latency
- Subclass 2
  - Supports deterministic latency using the ~SYNC signal only
  - Minimizes clock traces but more complex

JESD204B Subclass 1 Deterministic Latency



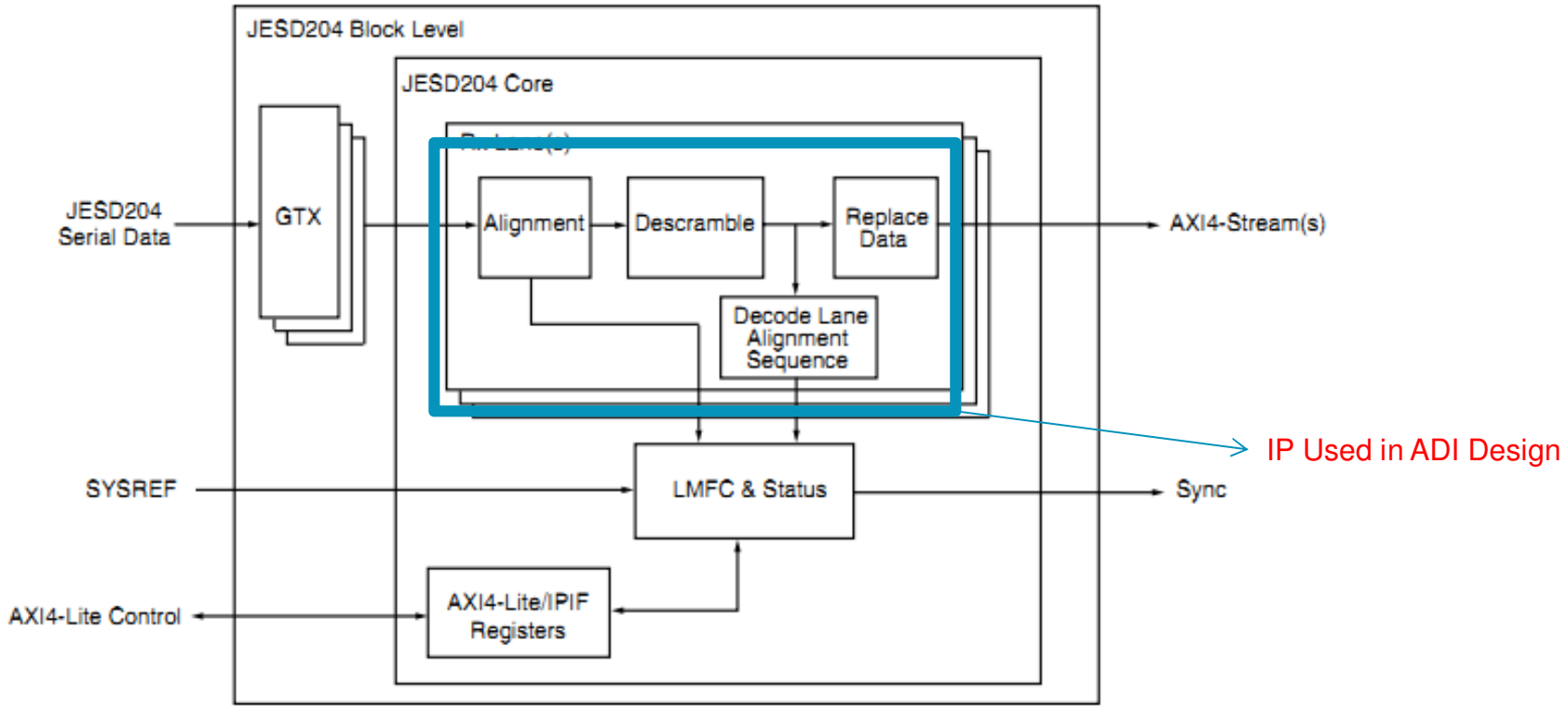
Xilinx JESD204B IP

Xilinx JESD204B IP (HDL)



- Supports Transmit, Receive, and Duplex (TX & RX)
- 1 to 12 lane configurations up to 12.5 Gbps
- Support for subclass 0, 1, and 2
- Deterministic latency for subclass 1 and 2
- AXI-4 Stream for data /AXI4-Lite for configuration

Xilinx JESD204B Receiver Architecture



- AXI4-Stream I/F per lane
- ILA capture per lane
- Alignment character detection and replacement per lane
- De-scrambling per lane
- LMFC state machine & Sync I/F
- Transceiver and block level wrappers

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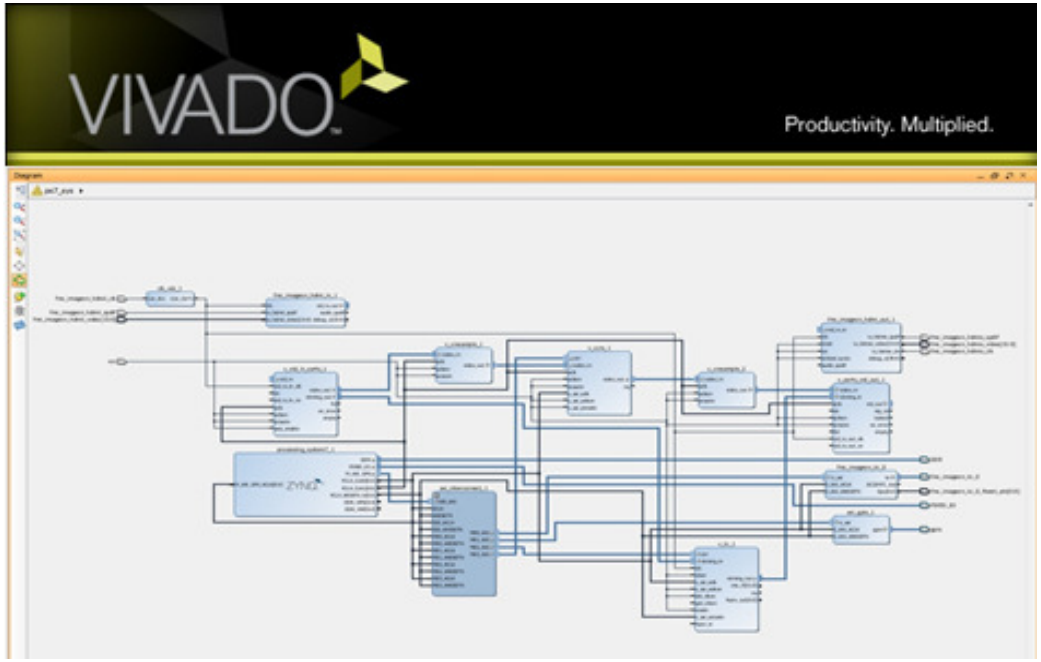
Designing with JESD204B in UltraScale

```
set axi_ad9144_jesd [create_bd_cell -type ip -vlnv xilinx.com:ip:jesd204:5.2 axi_ad9144_jesd]
 set_property -dict [list CONFIG.C_NODE_IS_TRANSMIT {1}] $axi_ad9144_jesd
 set_property -dict [list CONFIG.C_LANES {4}] $axi_ad9144_jesd
```

- Instantiate JESD204B component in TcL script

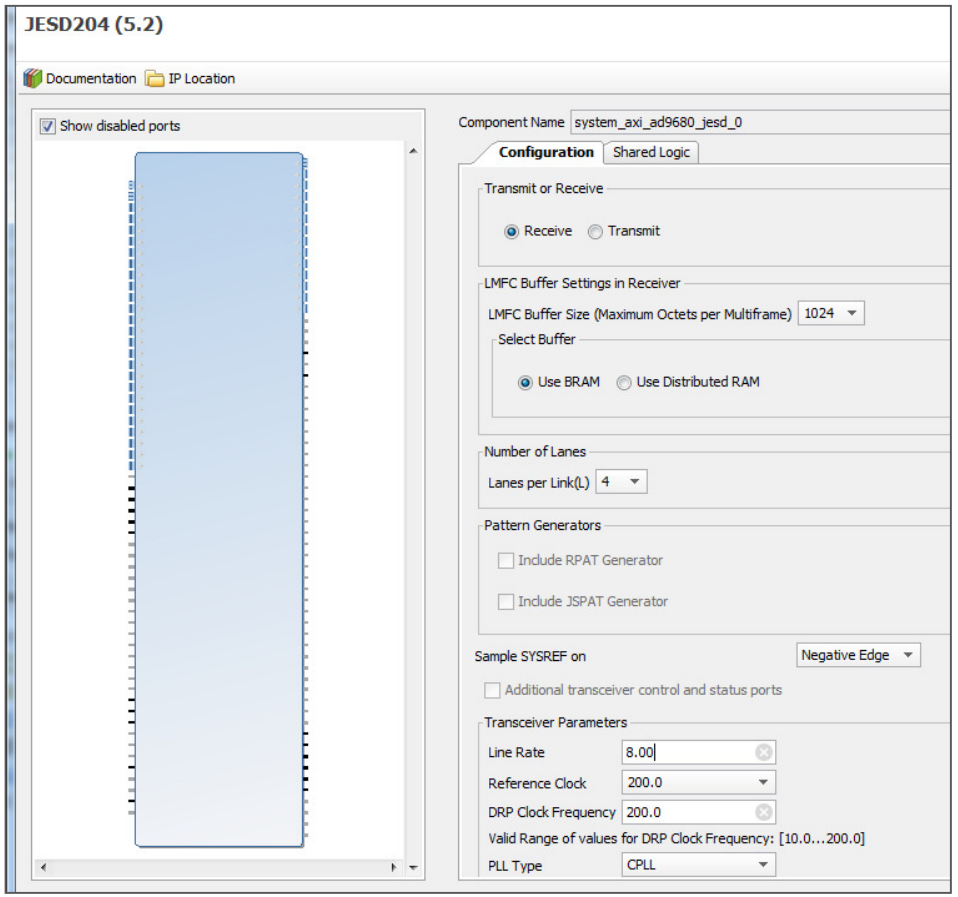


- Build Vivado project from TcL

Designing with JESD204B in UltraScale

- Customize in Vivado IP Integrator

- Number of lanes
- Line rate
- Shared Logic
  - Transceivers can be included ‘in core’, or ‘in example design’
- GT wizard automatically called as part of IP generation process



Xilinx JESD204B

JESD204 High Speed Interface

Docs

Key Documentation

- JESD204B IP Core Product Brief
- JESD204B IP Core Product Guide
- Interoperability Reports
- ADI JESD204B Survival Guide

Related Products

- Kintex-7 FPGA KC705 Evaluation Kit
- Zynq-7000 AP SoC ZC706 Evaluation Kit
- Virtex-7 FPGA VC707 Evaluation Kit
- Virtex-7 FPGA VC709 Connectivity Kit

Eval boards

JESD204B is poised to take over as the technology of choice for interfacing high speed data converters to FPGAs much the same way that LVDS interfaces began overtaking its predecessor CMOS.

The JESD204B interface standard supports the high bandwidth necessary to keep pace with today's leading high performance, high speed and multi-channel applications, while greatly reducing the number of digital IOs needed and thus easing board layout. Very high-speed ADCs that would have previously required a complex interface design using a large number of FPGA IO are now implemented with just a few pins. The total bandwidth of the JESD204B interface can also be separated into multiple channels based on the requirements of the application again without requiring additional pins.

JESD204B Benefits

Application	Key Benefit
Wireless	Supports high bandwidth with fewer pins to simplify layout
SDR	Support flexibility to dynamically adjust channel configurations
Medical Imaging	Supports high # of channels with fewer pins to simplify layout
Radar	Supports high bandwidth with fewer pins to simplify layout

Ref Designs & IP core

Quick Links

- JESD204B IP Core
- JESD204B Hardware Demos
- JESD204B Reference Designs

Partner links

Partner Solutions

- Analog Devices
- Texas Instruments
- IDT
- Intersil

Featured Videos

Rapid Prototyping with JESD204B using FMC and Xilinx FPGAs (1:35 min)

Video

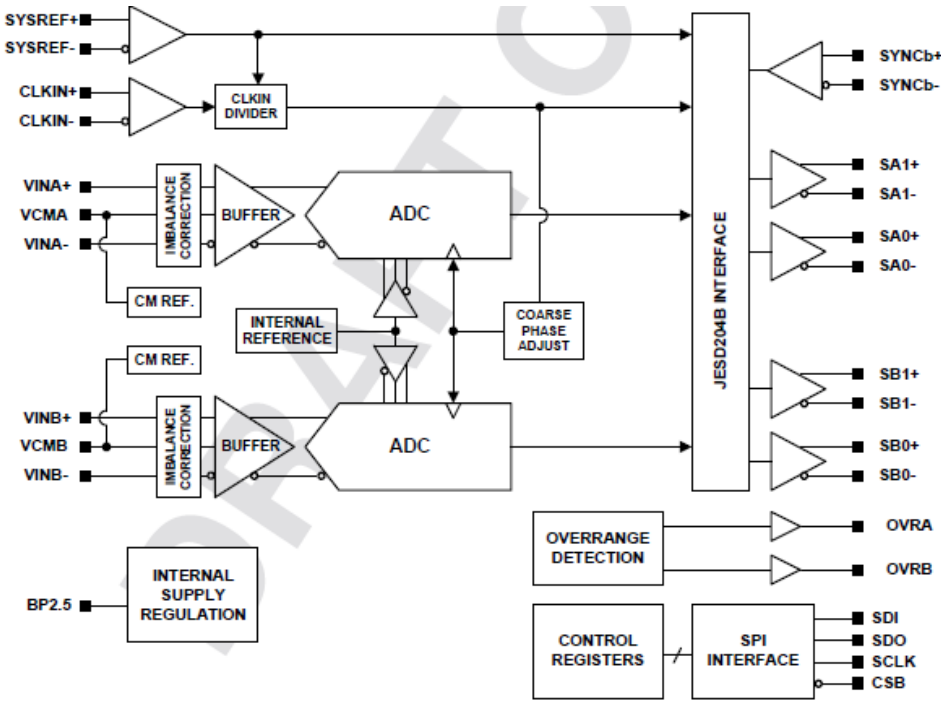
www.xilinx.com/JESD204

JESD204B Data Acquisition on Kintex UltraScale

ADC16DX370 2-channel, 16-bit, 370 MSPS ADC

- Low Power: 804mW/channel
- Input Clock Buffer /1 /2 /4 /8
- High Dynamic Range: @ 150MHz Input
  - NSD: -152.4 dBFS/Hz (69.7dB SNR)
  - SFDR : 88 dBFS
- Up to 185MHz information bandwidth
- JESD204B Subclass 1
  - Single Lane/ADC up to 7.4Gbps
  - Dual Lane/ADC up to 3.7Gbps

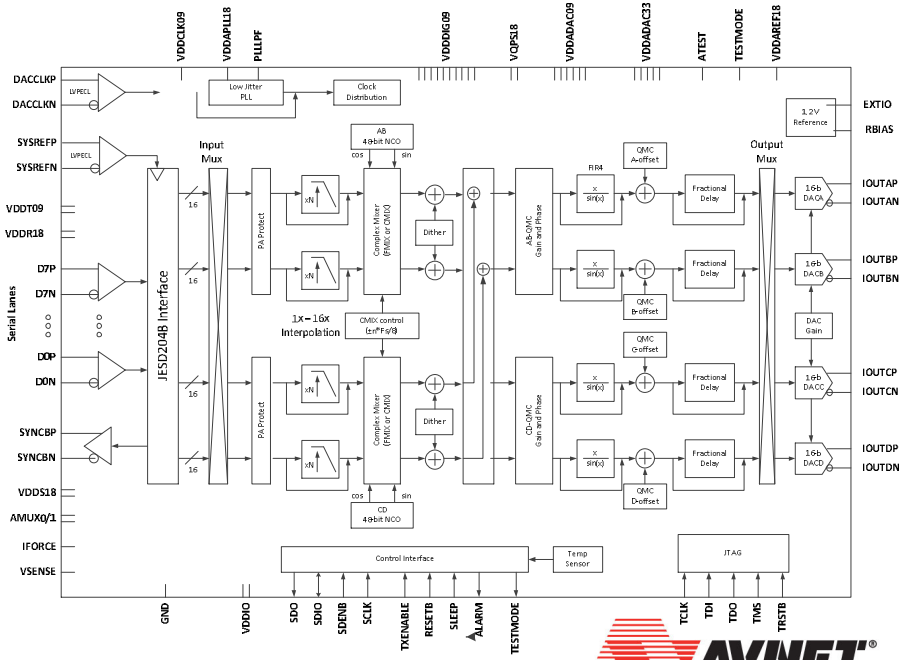
- Applications
  - 3G/4G/GSM Diversity RX or TX DPD
  - SIGINT, RADAR, EW, ELINT
  - Spectrum Analyzer, Wireless Test



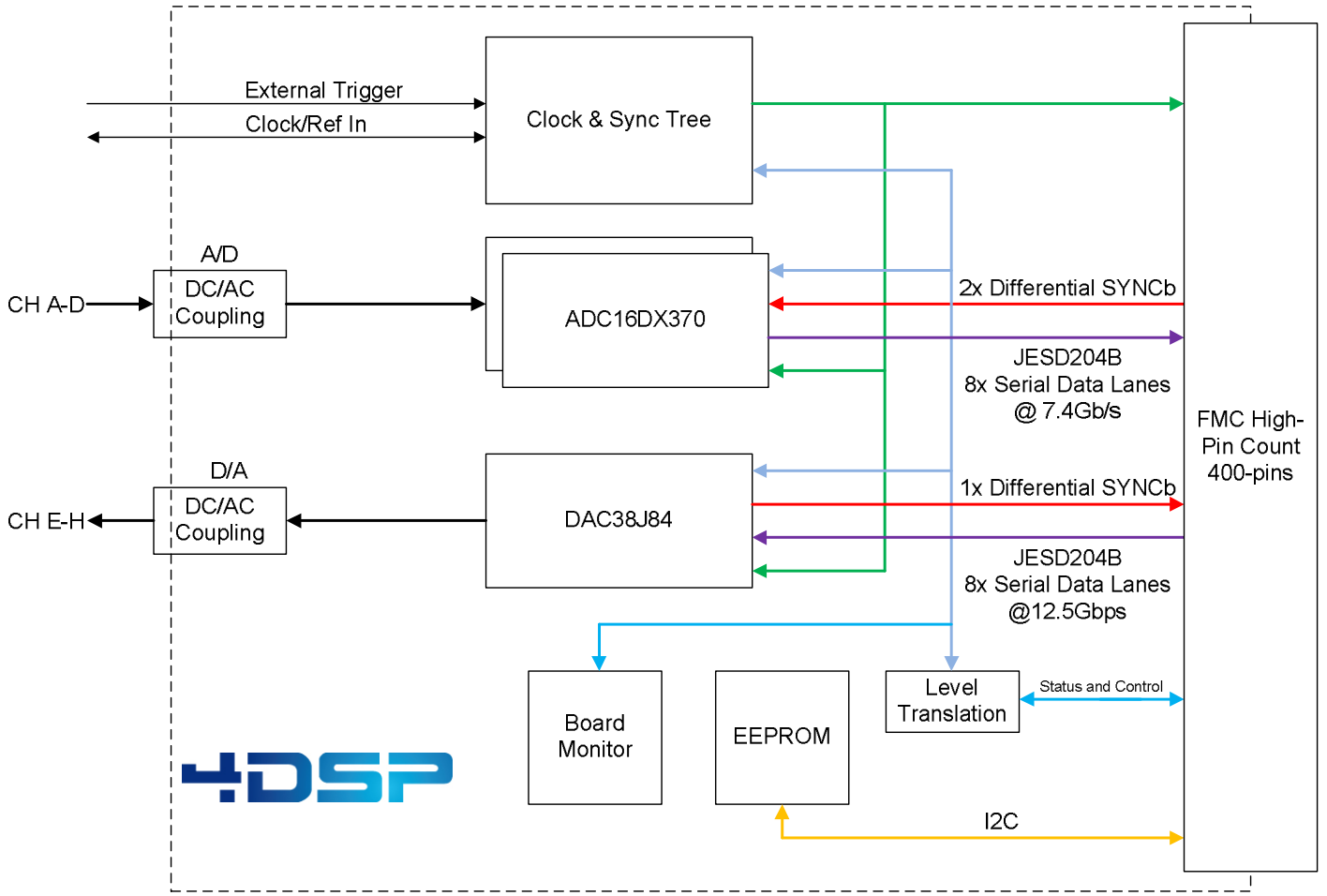
DAC38J84, DAC37J84 Quad 16-bit, 2.5/1.6 GSPS DAC

- 400 mW/ch @ 2.5GSPS, 275 mW/ch @ 1.6GSPS
- Multi-DAC Synchronization
- 1x -16x interpolation
- 2 complex mixers with 48-bit NCOs
- Power measurement with PA protection
- JESD204B 12.5 Gbps
  - Up to 8 lanes

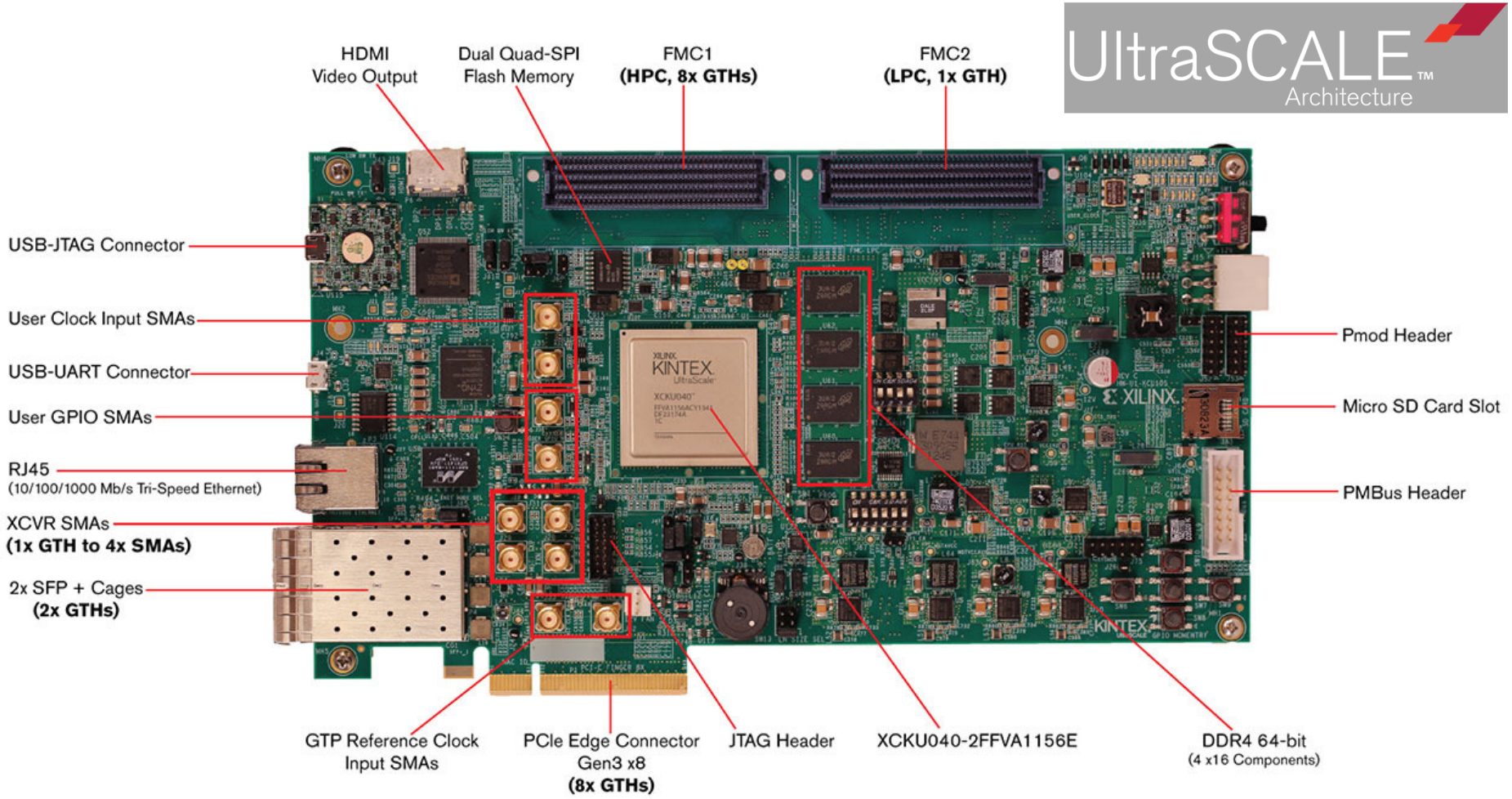
- Applications
  - Wireless Infrastructure
  - Wireless Backhaul
  - Point-to-Point Microwave
  - Software Defined Radio
  - Test and Measurement



Texas Instruments / 4DSP FMC144



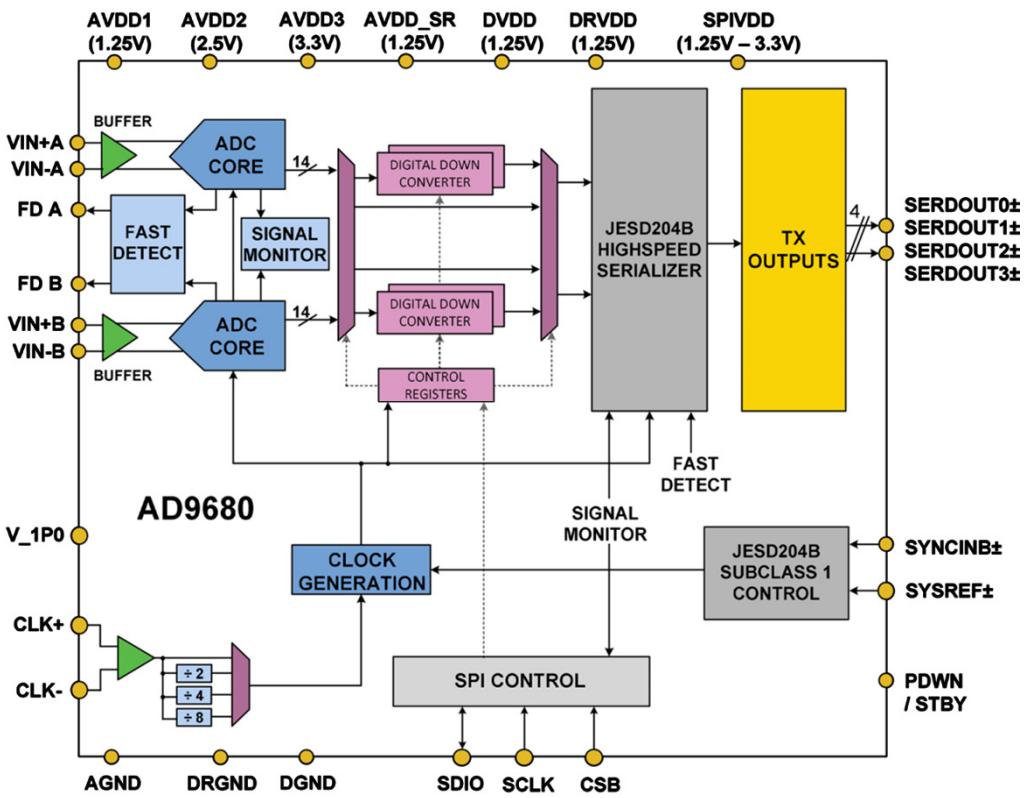
Xilinx Kintex UltraScale KCU105 Development Board



- Available Q2/15

AD9680-1000 Dual Channel 14-bit 1GSPS ADC

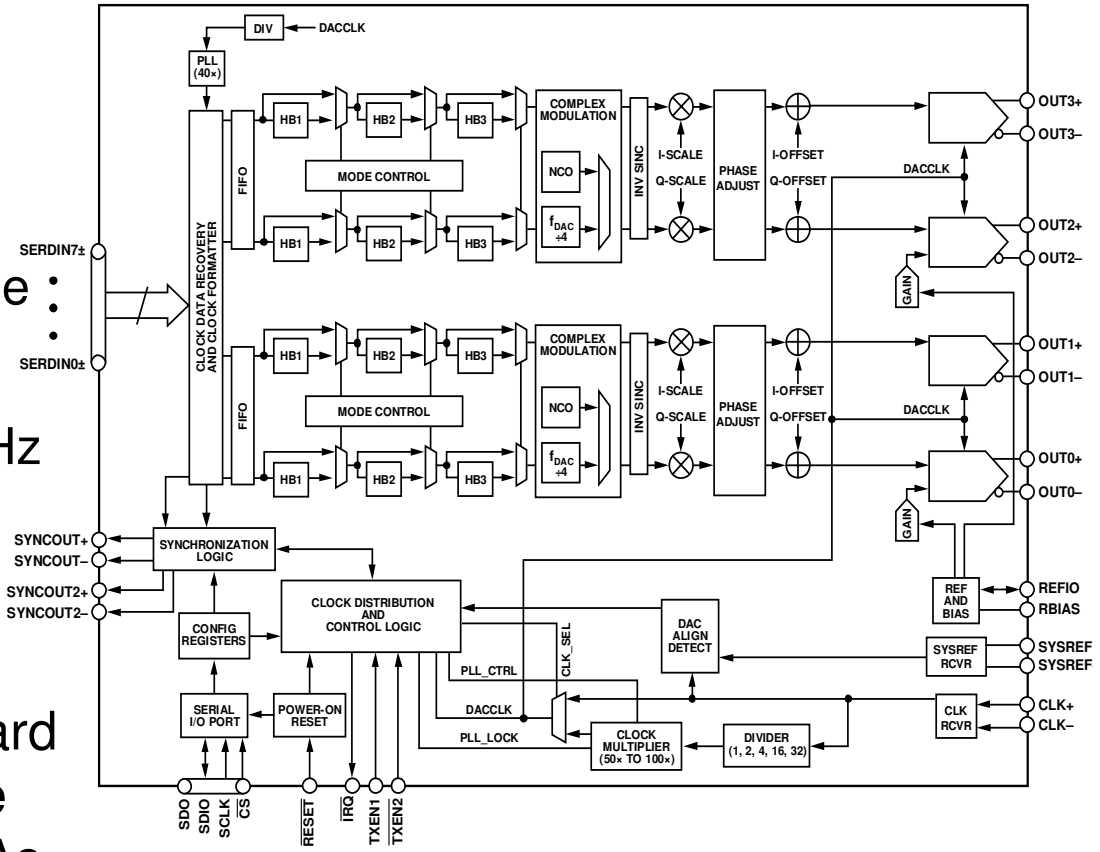
- Wide full-power bandwidth
  - IF sampling ≤ 2 GHz
- Programmable buffered inputs
- Four wide-band decimation filter and NCO blocks
  - Supports multi-band receivers
- Programmable fast over range detection and signal monitoring
- Configurable JESD204B interface



www.analog.com/AD9680

AD9144 16-bit 2.8 GSPS Quad DAC

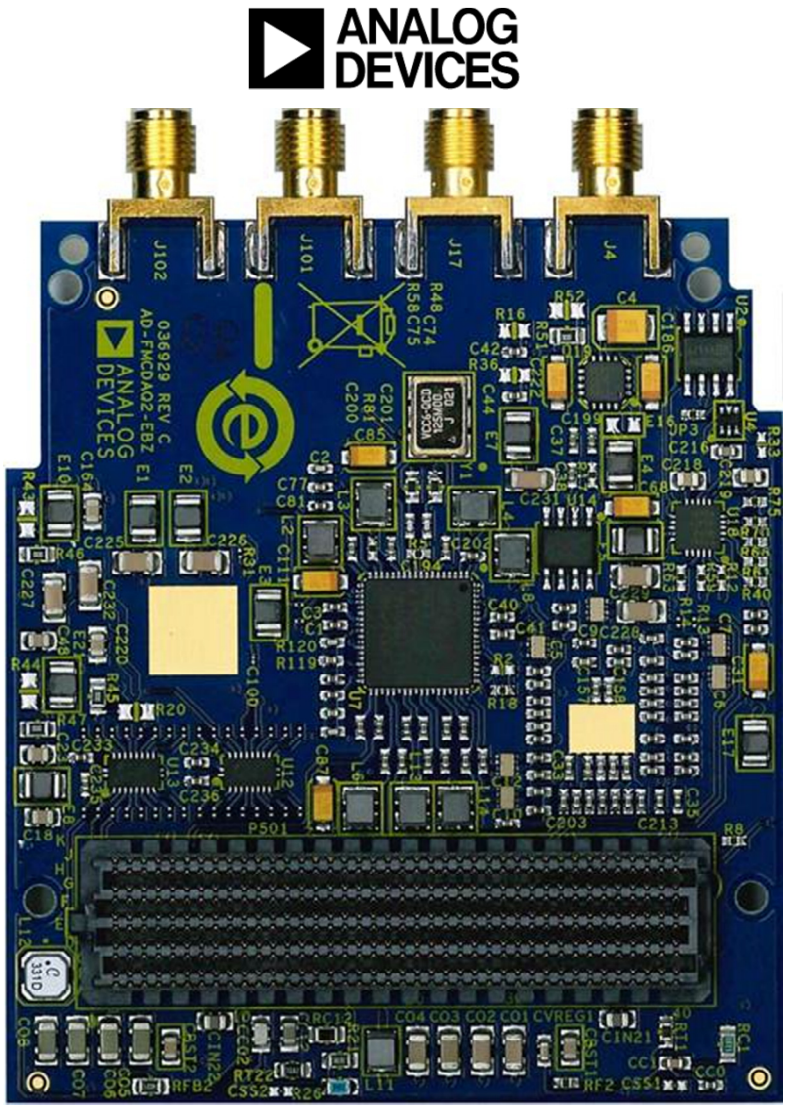
- 2.8 GSPS DAC Update Rate
  - Eases filtering of spectral images
- Low Noise Spectral Density
  - -164 dBm/Hz @ 150 MHz Fout
  - Enables high dynamic range
- Spurious Performance
  - SFDR = -76 dBc @ 150 MHz Fout
  - IMD = -82 dBc @ 150 MHz Fout
- 8 JESD204B lanes ease board layout congestion and enable efficient connections to FPGAs



www.analog.com/AD9144

Analog Devices FMCDAQ2 JESD204B

- Dual Channel 14-bit 1GSPS ADC (AD9680-1000)
- 16-bit 2.8 GSPS Quad DAC (AD9144, 2 channels connected)
- JESD204B Subclass 1 deterministic latency for channel synchronization
- Requires HPC-FMC (8 lanes of GTH)
- Reference designs for Xilinx / Avnet baseboards
  - UltraScale KCU105
  - Avnet Mini-ITX
  - ZC706
  - KC705



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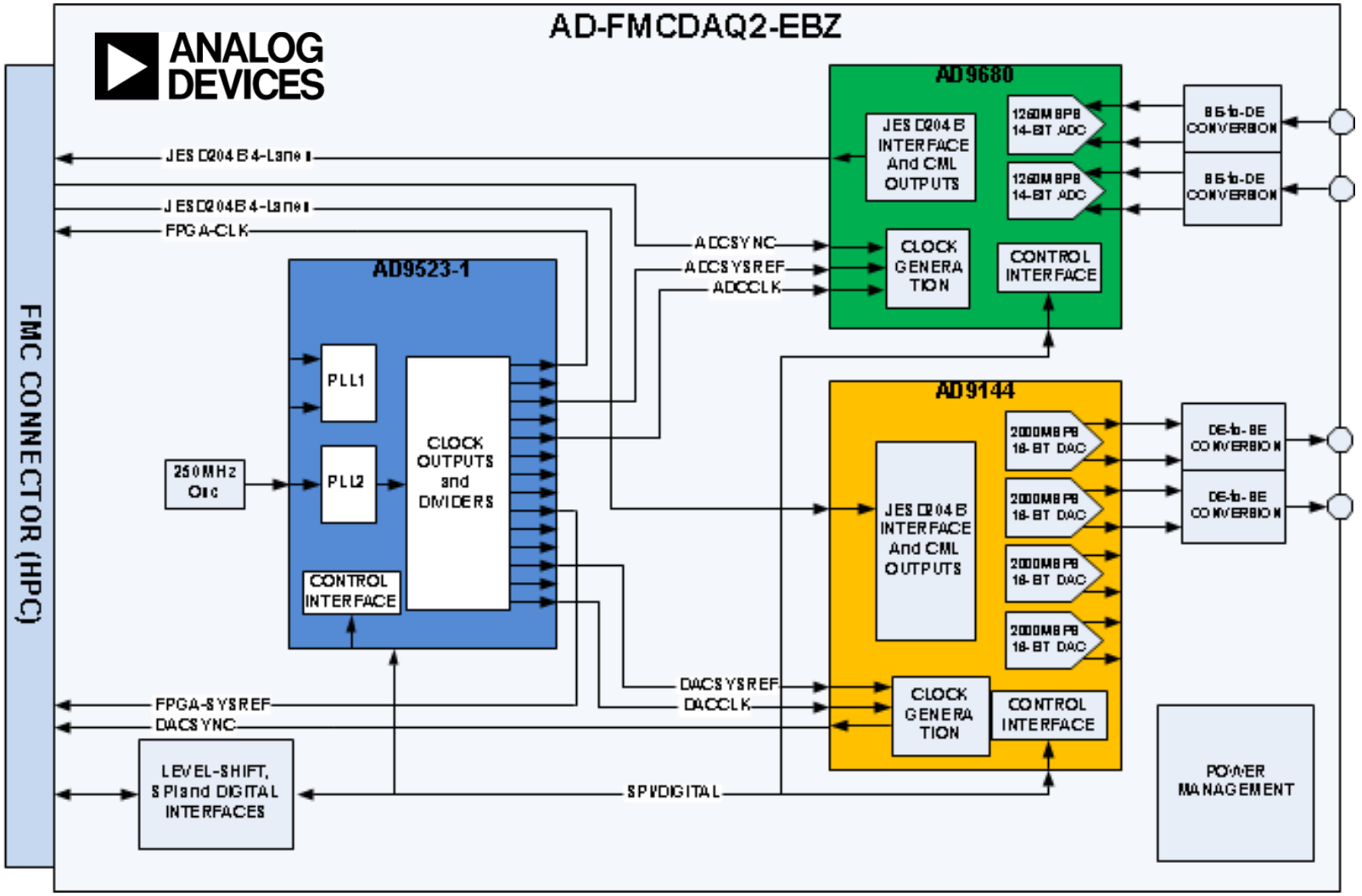
Analog Devices FMCDAQ2 JESD204B



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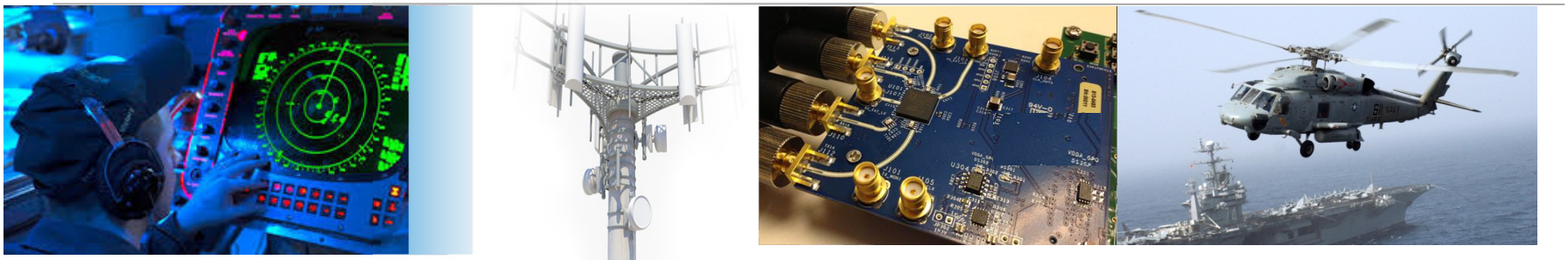
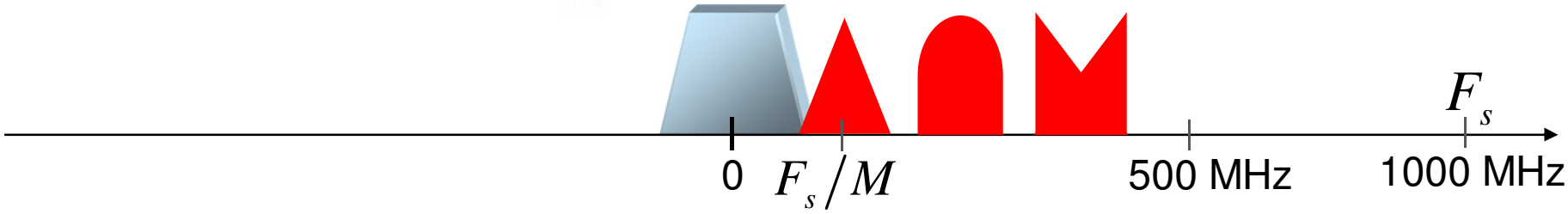
Digital Signal Processing for WideBand Data Acquisition

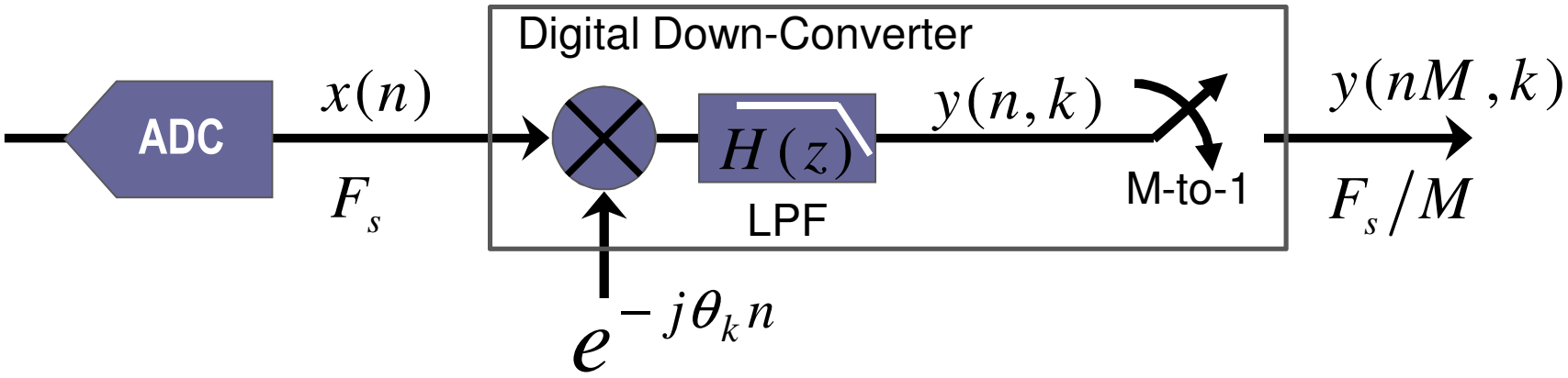
With JESD204B High-Speed Data Converters

Digital Down-Converter

...







- Extract the channel of interest and reduce sampling rate for downstream processing

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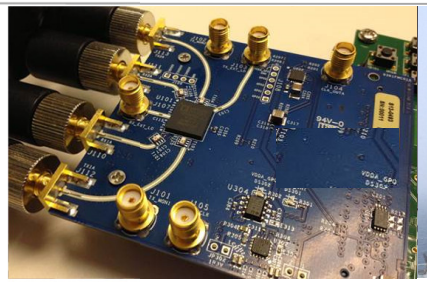
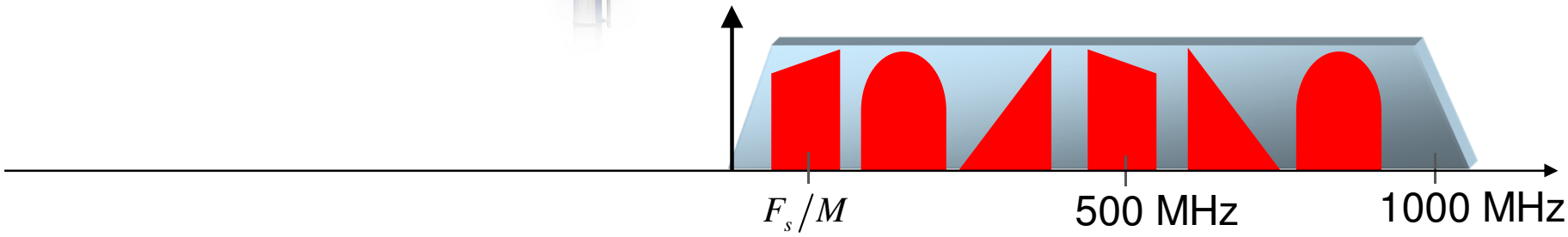
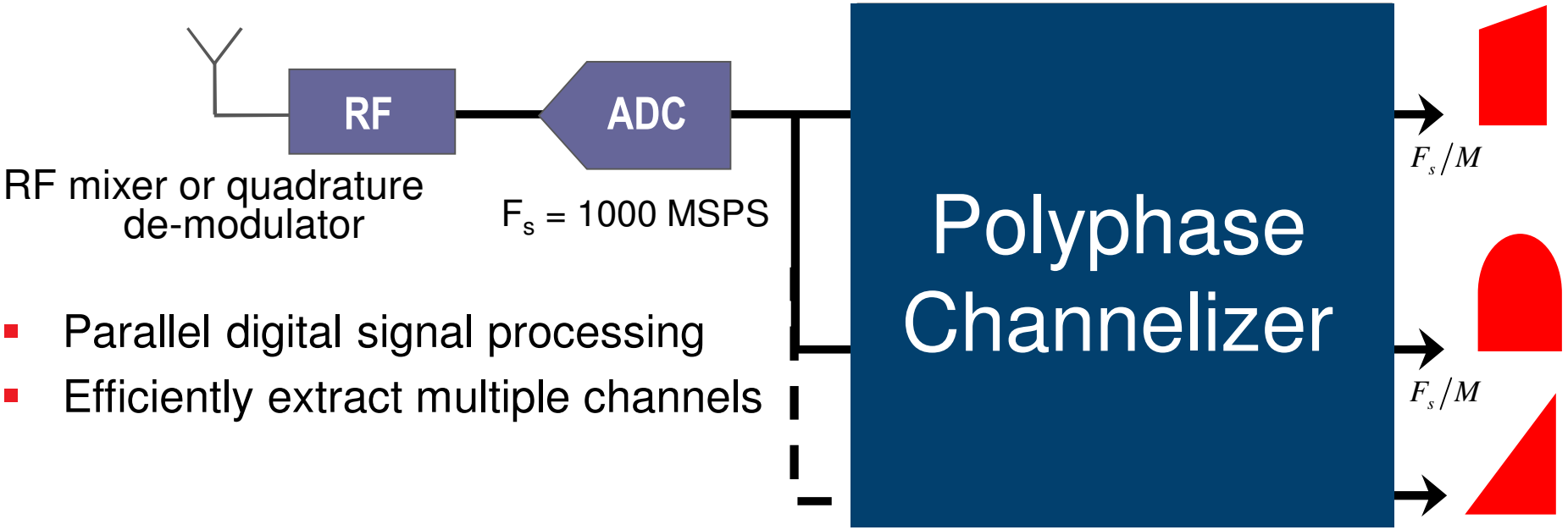
Digital Signal Processing for Multi Channel



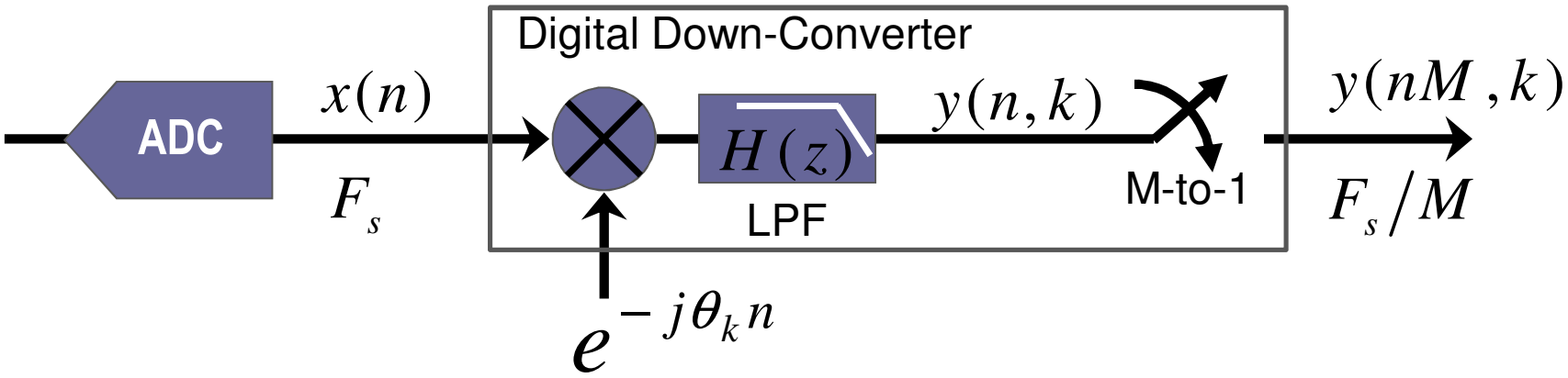


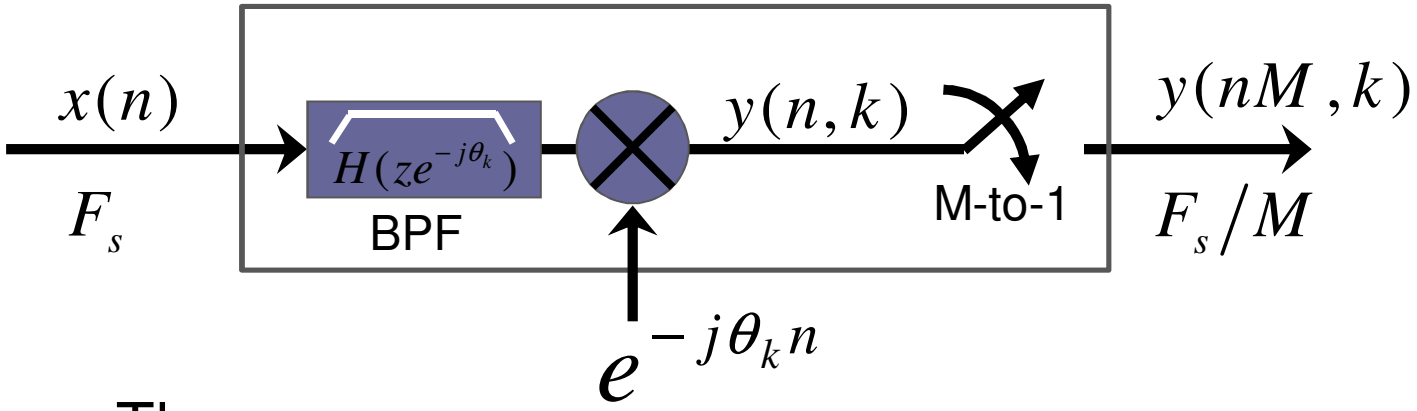


- Parallel digital signal processing
- Efficiently extract multiple channels

Analysis and Construction of Polyphase Channelizer



- Start with standard digital down-converter, one / channel



- Equivalency Theorem
  - Heterodyne + baseband filter = bandpass filter + heterodyne

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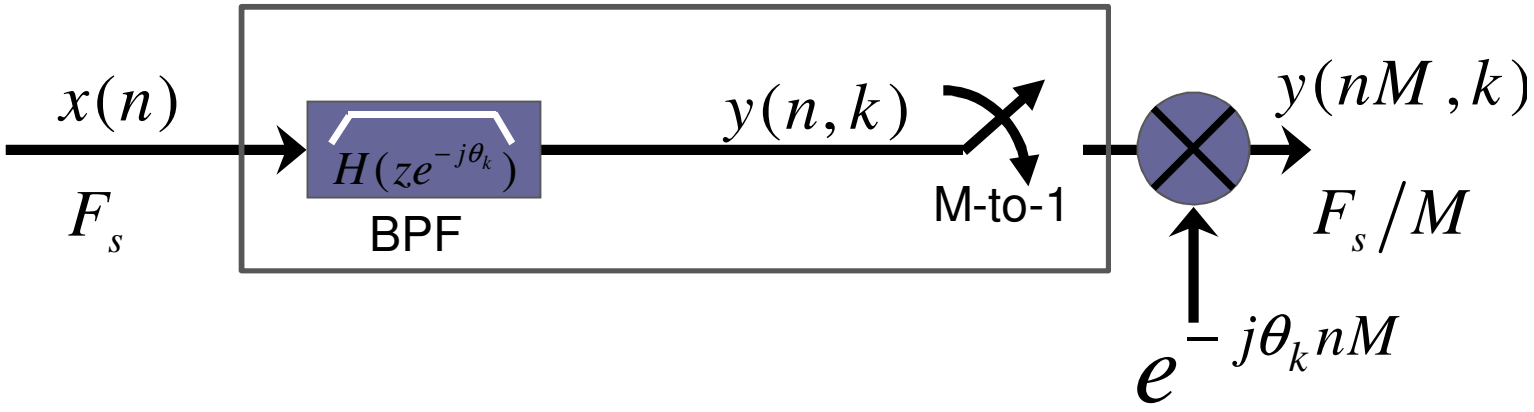
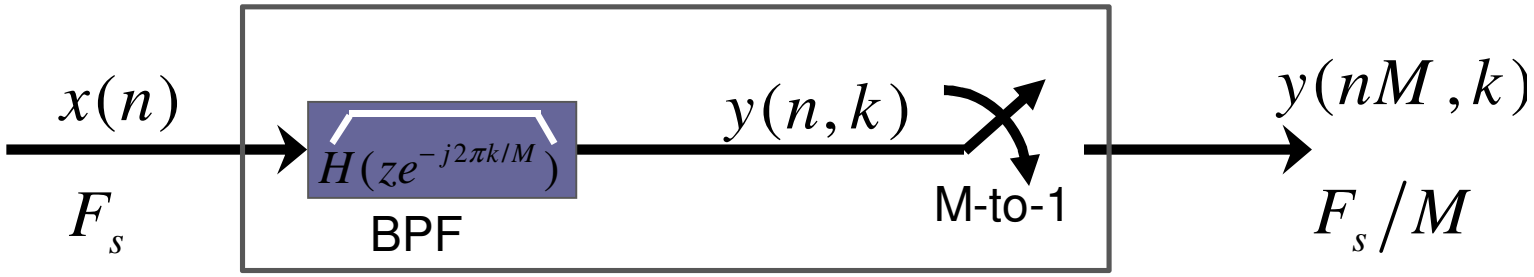
Analysis and Construction of Polyphase Channelizer



- Slide heterodyne through downsampler
- Select $\theta_k = 2\pi k / M \Rightarrow e^{-j\theta_k nM} = e^{-j2\pi kn} = 1$



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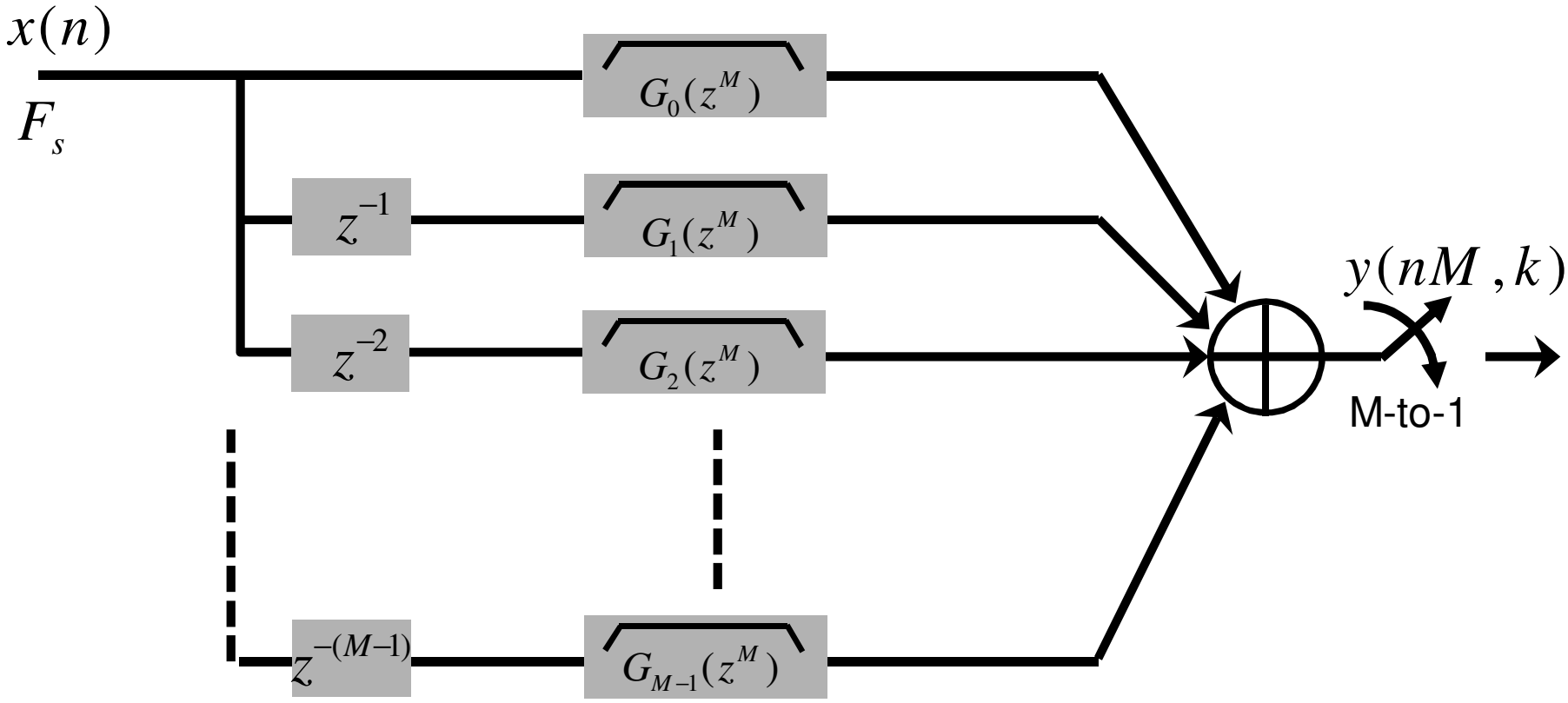
Analysis and Construction of Polyphase Channelizer

- Create polyphase partition



where $G(z) = H(ze^{-j2\pi k/M})$

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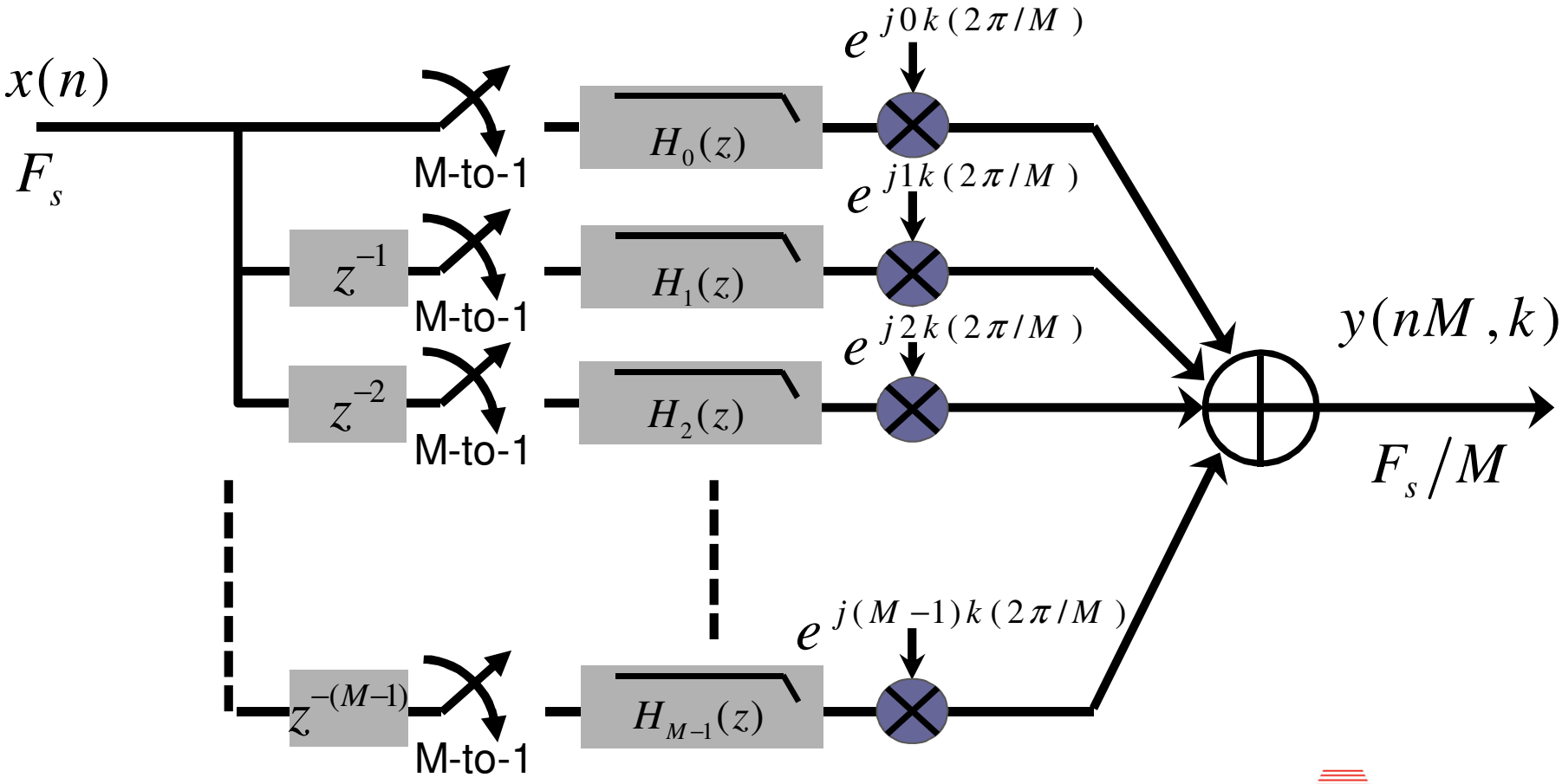
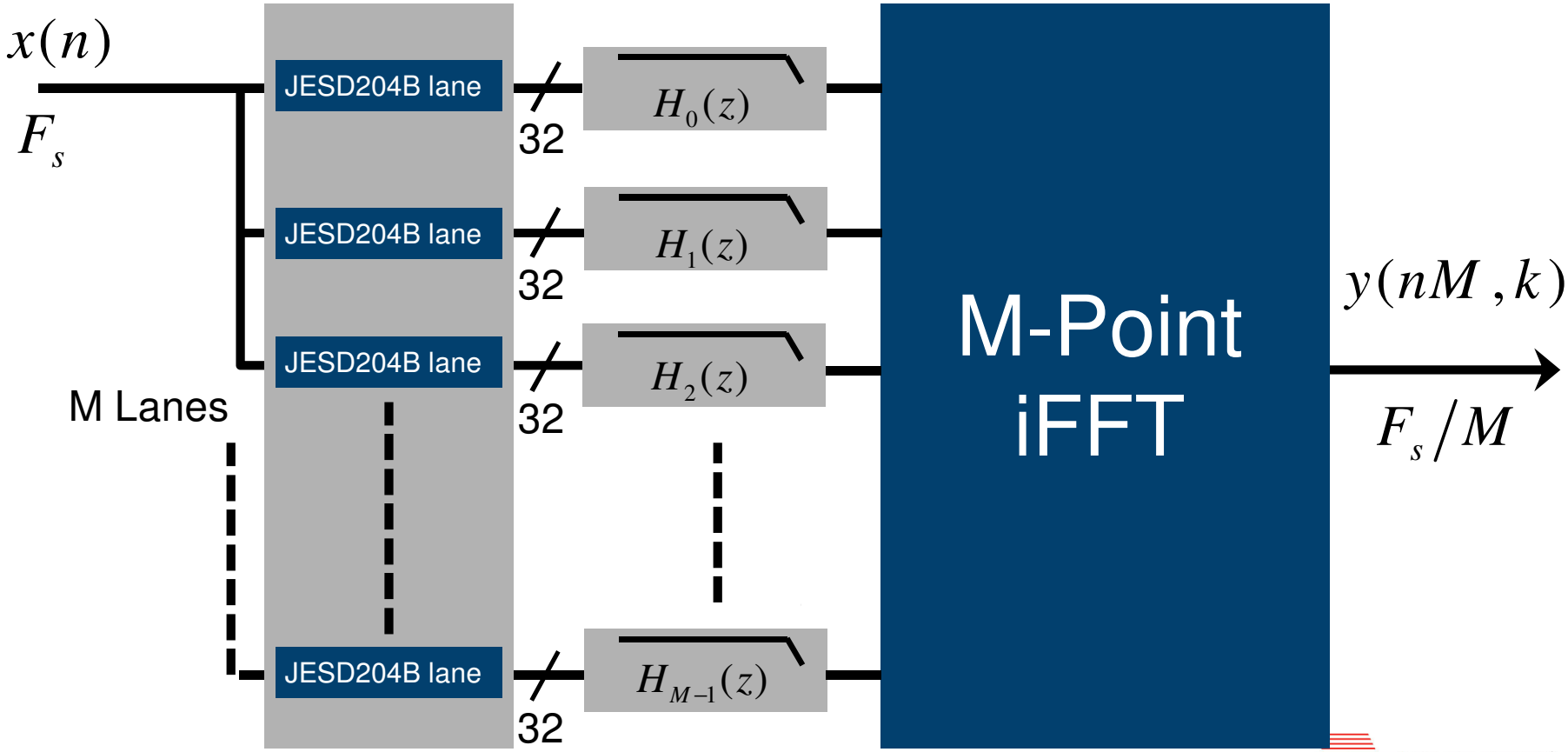
Analysis and Construction of Polyphase Channelizer

- Apply Noble Identity to each sub-filter
- Decimation occurs ahead of sub-filters, operate at lower rate

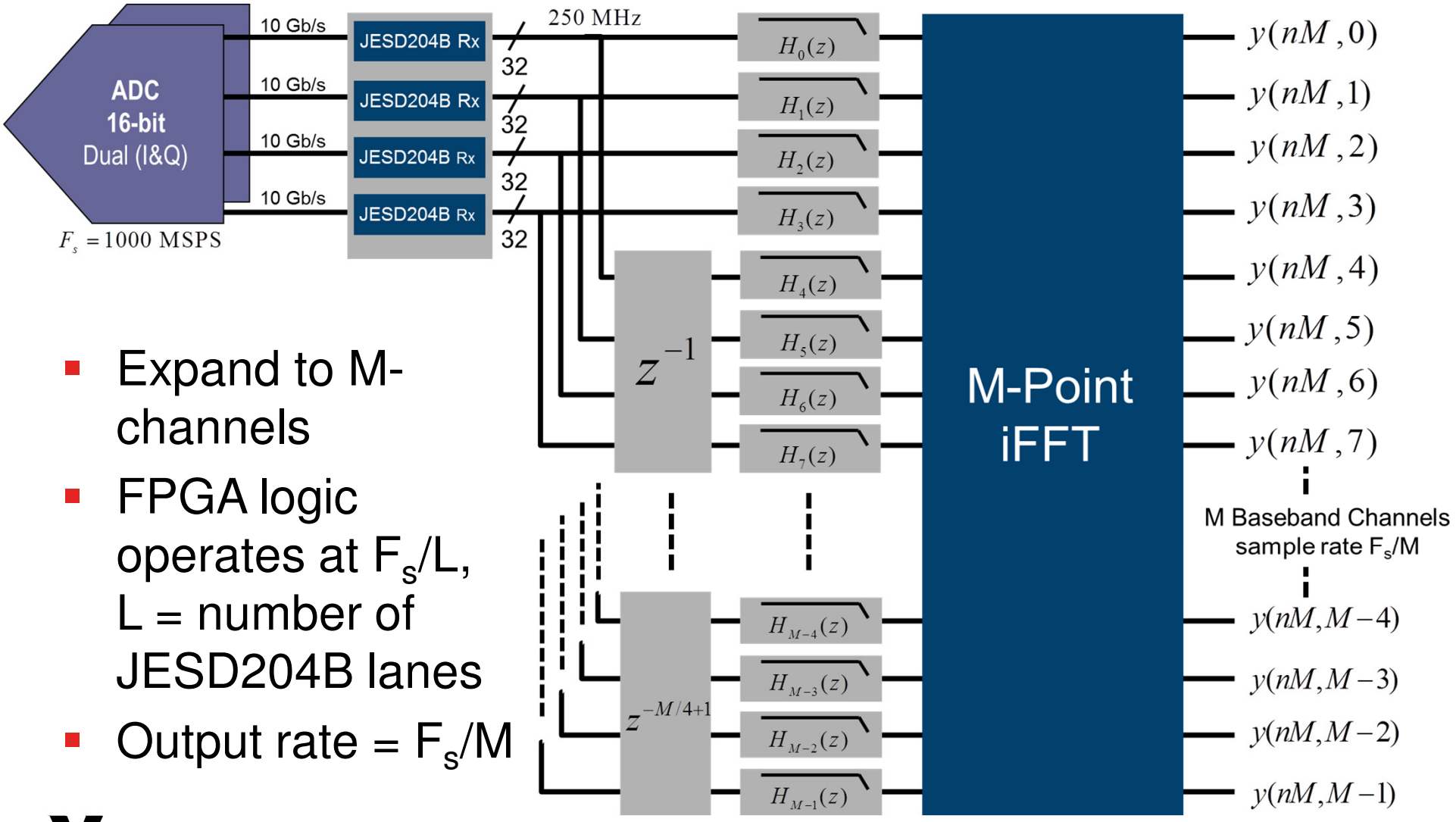


Analysis and Construction of Polyphase Channelizer

- Each JESD204B lane has 4-byte interface
- Multiple lanes present data in parallel at core clock rate

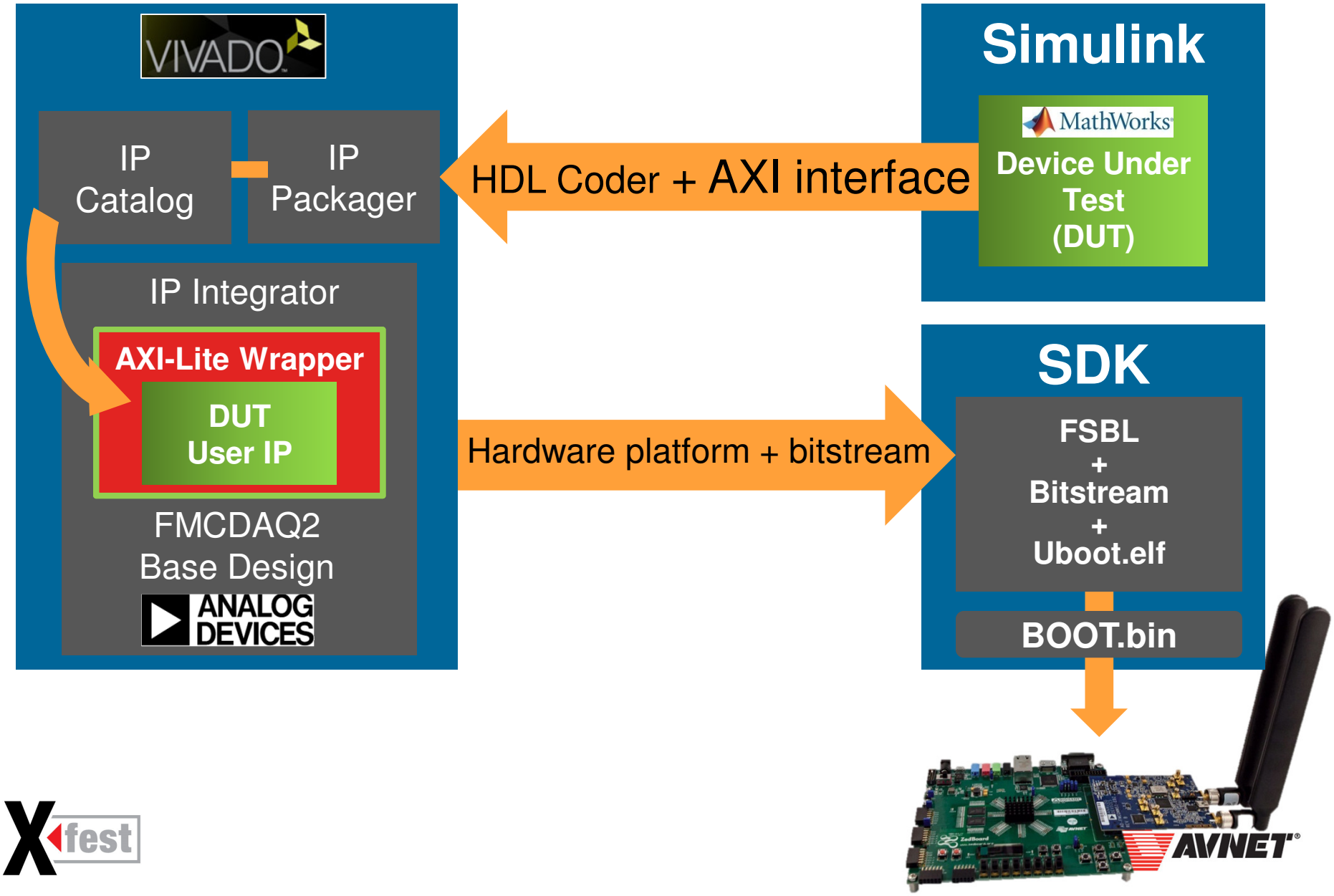


M-Channel Polyphase Channelizer over 4 JESD204B Lanes



- Expand to M-channels
- FPGA logic operates at F_s/L, L = number of JESD204B lanes
- Output rate = F_s/M

Design Flow for Digital Signal Processing



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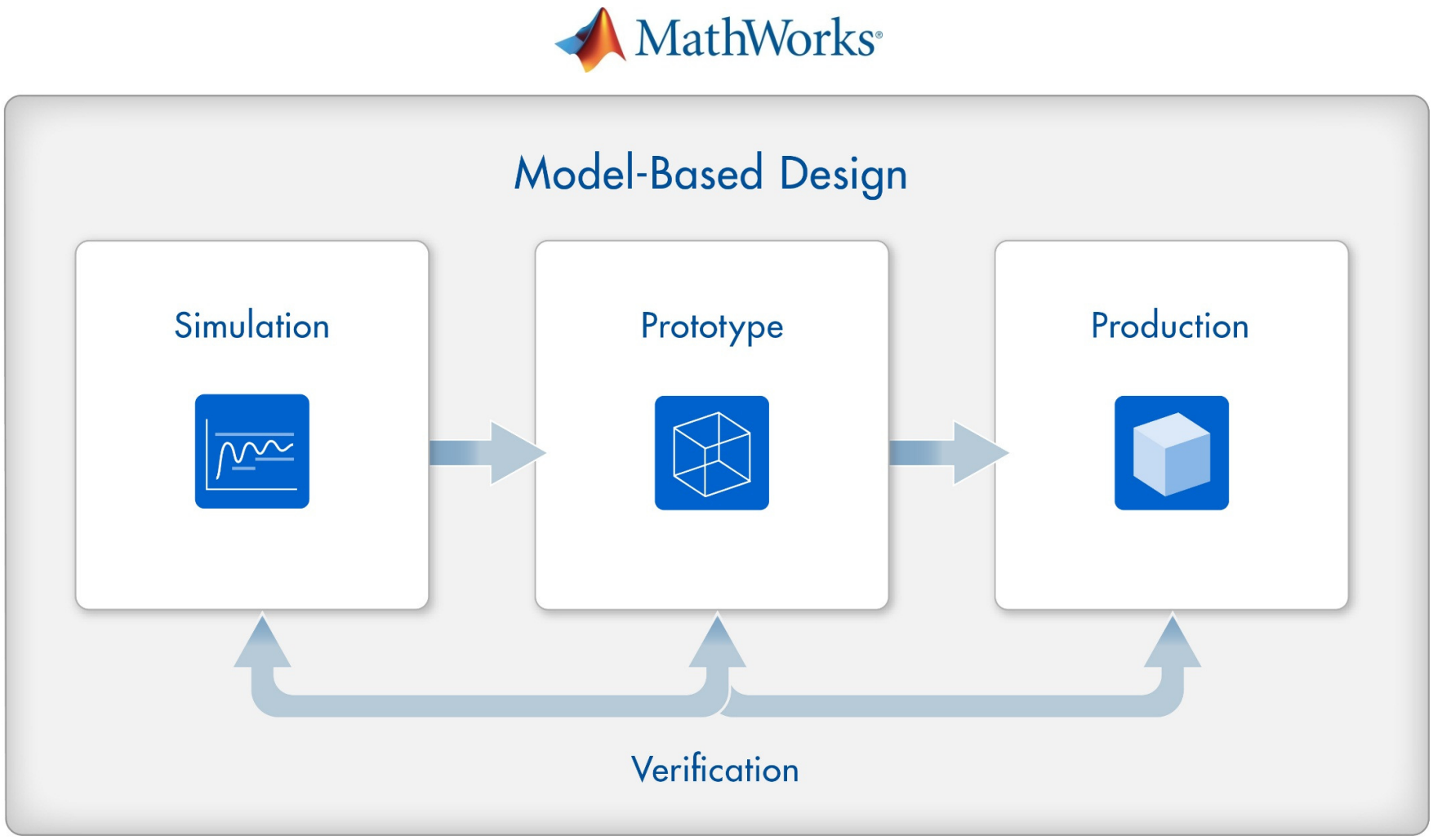
Model-Based Design with MATLAB and Simulink



What is Model-Based Design?

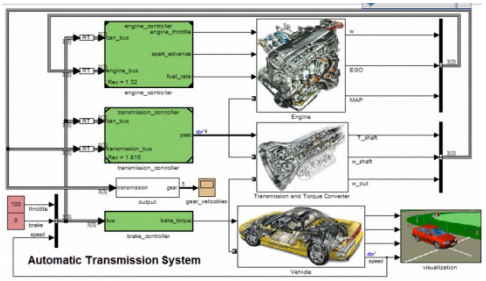
Model-Based Design (From Wikipedia, the free encyclopedia)

Model-Based Design (MBD) is a ***mathematical*** and ***visual method*** of addressing problems associated with designing complex control, signal processing and communication systems.

Model-Based Design according to MathWorks website

Model-Based Design is transforming the way engineers and scientists work by moving design tasks from the lab and field to the desktop. When organizations adopt Model-Based Design, they ***improve product quality and reduce development time by 50% or more.***

From model

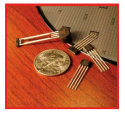


Automatic Code Generation

MATLAB/SimuLink Coder
HDL coder

Product

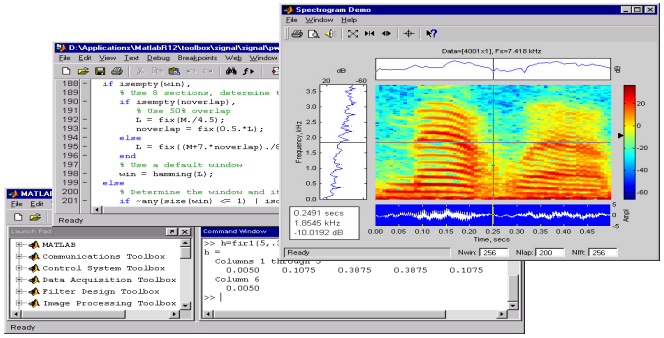
C and C++ code
HDL code for FPGA
Working production system



Model-Based Design Tools

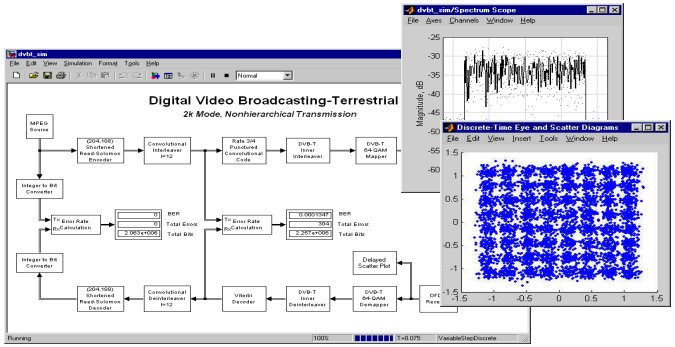
MATLAB®

The leading environment for technical computing



SIMULINK®

The leading environment for modeling, simulating, and implementing dynamic and embedded systems



XILINX SYSTEM GENERATOR™ For DSP

Embedded Coder®

HDL Coder™

Toolboxes
(signal, comms, etc.)

SIMULINK®

MATLAB®

MathWorks Design Package for Xilinx Kits

- Develop advanced communications systems on Xilinx FPGAs and SoC with tools for algorithm development and simulation along with code generation for C and HDL

Algorithm Design and Simulation

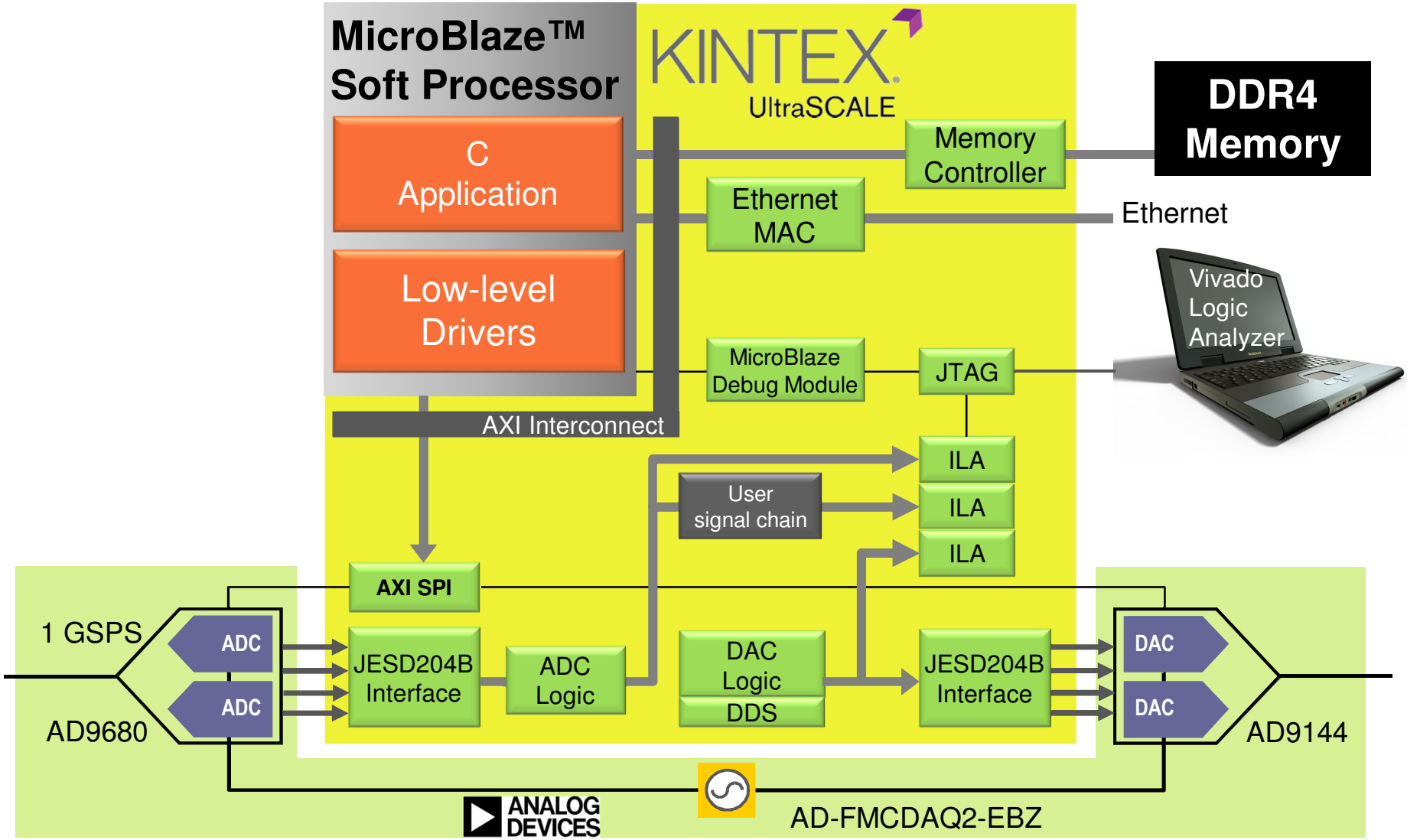
- MATLAB
- Simulink
- Fixed-Point Designer™
- Signal Processing Toolbox™
- DSP System Toolbox™
- Communications System Toolbox™

Code Generation for C and HDL

- MATLAB Coder™
- Simulink Coder™
- Embedded Coder®
- HDL Coder™

http://www.em.avnet.com/en-us/design/drc/Pages/Zynq-7000-AP-SoC--AD9361-Software-Defined-Radio-Evaluation-Kit.aspx

Data Acquisition with JESD204B in Xilinx UltraScale



Summary

- Xilinx UltraScale features for wideband data acquisition
- JESD204B data converter high-speed serial interface
- Xilinx JESD204B IP
- JESD204B data acquisition on Kintex UltraScale
- Digital signal processing for wideband data acquisition

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Juspaxar
Mochchakkeram
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Tingki
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Gratias Tibi
Obrigado
Ua Tsaug Rau Koj
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Grazas
cảm ơn bạn
Kia Ora
Kop Khun
Děkuji
Nirringrazzjak
Di Ou Mèsi
Suksama
Nuwun
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Matur
Misaotra
Hvala
Welalin
Djiere Dieuf
Danke
Merci
Go Raibh Maith Agat
Eskerrik Asko
Salamat
Najis Tuke

Appendix

Equivalency Theorem

$$y(n,k) = [x(n)e^{-j\theta_k n}] * h(n)$$

$$= \sum_{r=0}^{N-1} x(n-r)\, e^{-j(n-r)\theta_k} h(r)$$

$$= \sum_{r=0}^{N-1} x(n-r)\, e^{-jn\theta_k} h(r) e^{jr\theta_k}$$

$$= e^{-jn\theta_k} \sum_{r=0}^{N-1} x(n-r)\, h(r) e^{jr\theta_k}$$

- Heterodyne and low pass filter same as band pass filter and heterodyne

UltraScale Architecture DSP vs. 7 series DSP

Function	7 Series	UltraScale
DSP Tile/Slice Type	DSP48E1	**DSP48E2**
Multiple Add/Sub/Acc operations	√	√
Multiplier and MACC	25x18	**27x18(19*)**
Squaring: [(A or B) +/- D]^2	**N/A**	√
WMUX feedback Ultra Efficient Complex Multiply CMACC	**6 x DSP48E1**	**3 x DSP48E2**
SIMD Support	√	√
Integrated Pattern Detect Circuitry	√	√
Integrated Logic Unit	√	√
Wide Mux functions (48 bit)	√	√
Wide XOR (96 bit)	**N/A**	√
Optional 96-bit output	√	√
Cascade routing	√	√
Pipeline registers	√	√
D Pre-adder	√	√
Sequential complex multiply, AB dyn access	√	√
AB register pipeline balancing improved	√	√

* Uses the C-input to add one more bit

Kintex and Virtex UltraScale 20nm Capabilities

	KINTEX-7	KINTEX UltraSCALE	VIRTEX-7	VIRTEX UltraSCALE
Logic Cells (LC)	478	**1,161**	1,995	**4,407**
Block RAM (BRAM) (Mbits)	34	**76**	68	**115**
DSP-48	1,920	**5,520**	3,600	**2,880**
Peak DSP Performance (GMACs)	2,845	**8,180**	5,335	**4,268**
Transceiver Count	32	**64**	96	**104**
Peak Transceiver Line Rate (Gb/s)	12.5	**16.3**	28.05	**32.75**
Peak Transceiver Bandwidth (Gb/s)	800	**2,086**	2,784	**5,101**
PCI Express Blocks	1	**4**	4	**6**
Memory Interface Performance (Mb/s)	1,866	**2,400**	1,866	**2,400**
I/O Pins	500	**832**	1,200	**1,456**

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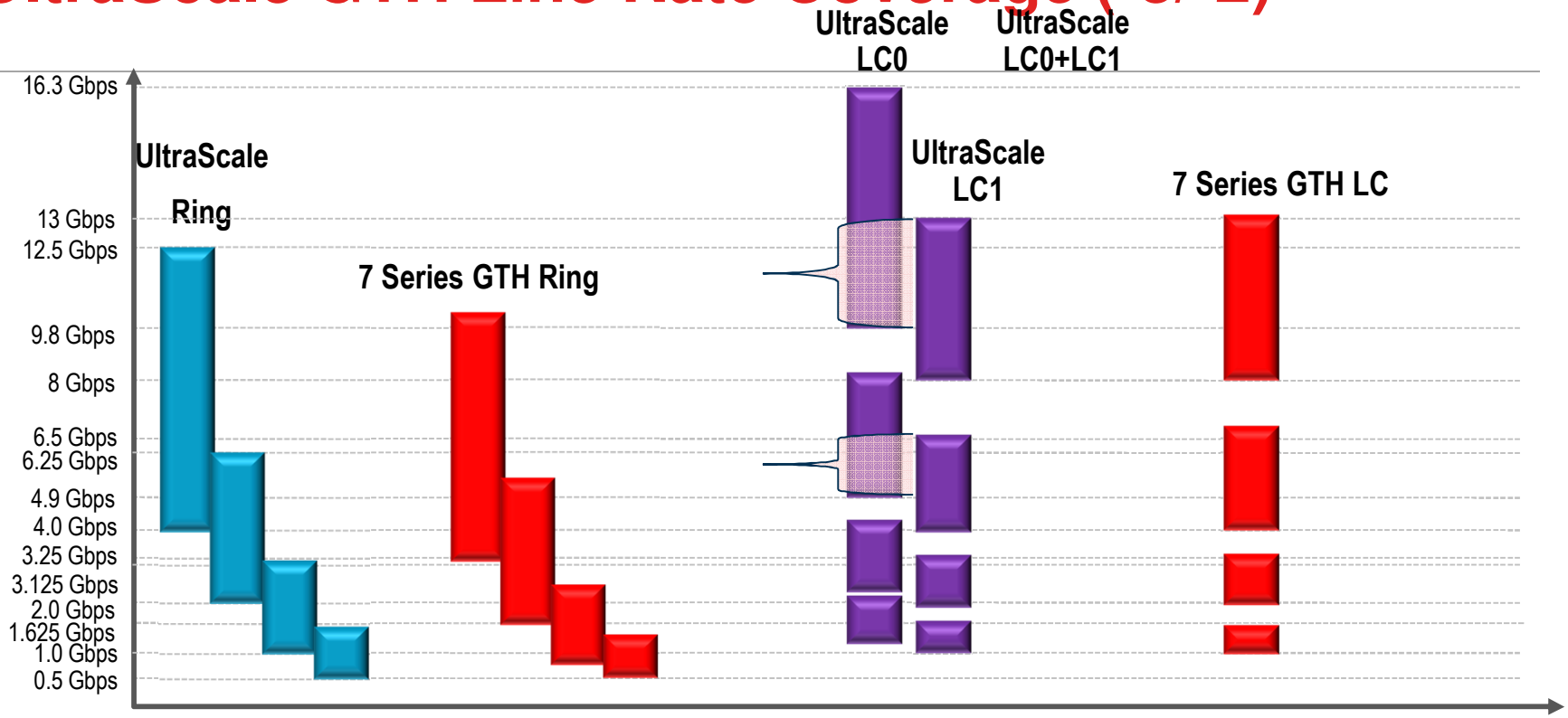
UltraScale GTH Line Rate Coverage (-3/-2)



Divider	UltraScale GTH			7 Series GTH	
	LC0	LC1-LB	Ring	LC	Ring
/1	9.8 – 16.3	8.0 – 13	4.0 – 12.5	8.0 – 13.1	3.2-10.3
/2	4.9 – 8.15	4.0 – 6.5	2.0 – 6.25	4.0 – 6.55	1.6-5.16
/4	2.45 – 4.075	2.0 – 3.25	1.0 – 3.125	2.0 – 3.25	0.8-2.58
/8	1.225 – 2.0375	1.0 – 1.625	0.5 – 1.5625	1.0 – 1.625	0.5-1.29

Note 1: /16 for LC is not shown for simplicity

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Kintex® UltraScale™ FPGAs

	Part Number	XCKU035	XCKU040	XCKU060	XCKU075	XCKU100	XCKU115
Logic Resources	CLB	25,391	30,300	41,460	54,000	68,460	82,920
	Logic Cells	355,474	424,200	580,440	756,000	958,440	1,160,880
	CLB Flip-Flops	406,256	484,800	663,360	864,000	1,095,360	1,326,720
Memory Resources	Maximum Distributed RAM (Kb)	5,908	7,050	9,180	7,290	12,825	18,360
	Block RAM/FIFO w/ECC (36 Kb each)	540	600	1,080	1,188	1,680	2,160
	Block RAM/FIFO (18 Kb each)	1,080	1,200	2,160	2,376	3,360	4,320
	Total Block RAM (Mb)	19.0	21.1	38.0	41.8	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	8	8	12	14	24	24
	I/O DLL	40	40	48	64	64	64
I/O Resources	Maximum Single-Ended HP I/Os	416	416	520	624	676	676
	Maximum Differential HP I/O Pairs	192	192	240	288	312	312
	Maximum Single-Ended HR I/Os	104	104	104	104	156	156
	Maximum Differential HR I/O Pairs	48	48	48	48	72	72
Integrated IP Resources	DSP Slices	1,700	1,920	2,760	2,592	4,200	5,520
	System Monitor	1	1	1	1	2	2
	PCIe® Gen1/2/3	2	3	3	4	6	6
	Interlaken	0	0	0	2	0	0
	100G Ethernet	0	0	0	1	0	0
	GTH 16 Gb/s Transceivers	16	20	32	52	64	64
Speed Grades	Commercial	-1	-1	-1	-1	-1	-1
	Extended	-2 -3	-2 -3	-2 -3	-2 -3	-2 -3	-2 -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2
	Package [1,2,3]	Dimensions (mm)	HR I/O, HP I/O, GTH 16 Gb/s				
Footprint Compatible with Virtex UltraScale	FBVA676[2]	27x27	104, 208, 16	104, 208, 16			
	FBVA900[2]	31x31	104, 364, 16	104, 364, 16			
	FFVA1156	35x35	104, 416, 16	104, 416, 20	104, 416, 28	104, 416, 28	
	FFVA1517[3] FLVA1517[3]	40x40			104, 520, 32	104, 520, 48	104, 520, 48
	FLVB1517	40x40					104, 260, 64
	FFVA1760[3] FLVA1760[3]	42.5x42.5				104, 624, 52	104, 624, 52
	FLVD1924	45x45					156, 676, 52
	FLVF1924	45x45					104, 624, 64

Virtex® UltraScale™ FPGAs

	Part Number	XCVU065	XCVU080	XCVU095	XCVU125	XCVU145	XCVU160	XCVU440
Logic Resources	CLB	44,760	55,714	67,200	89,520	102,500	115,800	314,820
	Logic Cells	626,640	780,000	940,800	1,253,280	1,435,000	1,621,200	4,407,480
	CLB Flip-Flops	716,160	891,429	1,075,200	1,432,320	1,640,000	1,852,800	5,037,120
Memory Resources	Maximum Distributed RAM (Kb)	4,230	3,980	4,800	8,460	9,480	10,710	28,710
	Block RAM/FIFO w/ECC (36 Kb each)	1,260	1,421	1,728	2,520	2,787	3,276	2,520
	Block RAM/FIFO (18 Kb each)	2,520	2,842	3,456	5,040	5,574	6,552	5,040
	Total Block RAM (Mb)	44.3	50.0	60.8	88.6	98.0	115.2	88.6
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	16	16	20	24	26	30
	I/O DLL	40	64	64	80	96	104	120
	Fractional PLL	5	8	8	10	13	13	0
I/O Resources	Maximum Single-Ended HP I/Os	468	780	780	936	988	988	1,404
	Maximum Differential HP I/O Pairs	216	360	360	432	456	456	648
	Maximum Single-Ended HR I/Os	52	52	52	104	52	52	52
	Maximum Differential HR I/O Pairs	24	24	24	48	24	24	24
Integrated IP Resources	DSP Slices	600	672	768	1,200	1,365	1,560	2,880
	System Monitor	1	1	1	2	3	3	3
	PCIe® Gen1/2/3	2	4	4	4	4	4	6
	Interlaken	3	6	6	6	9	9	0
	100G Ethernet	3	4	4	6	7	7	3
	GTH 16 Gb/s Transceivers	20	32	32	40	52	52	48
	GTY 33 Gb/s Transceivers	20	32	32	40	52	52	0
Speed Grades	Commercial	-1	-1	-1	-1	-1	-1	-1
	Extended	-2 -3	-2 -3	-2 -3	-2 -3	-2 -3	-2 -3	-2 -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2

	Package [1,2]	Dimensions (mm)	HR I/O, HP I/O, GTH 16 Gb/s, GTY 33 Gb/s						
Footprint Compatible with Kintex UltraScale	FFVC1517	40x40	52, 468, 20, 20	52, 468, 24, 24	52, 468, 24, 24				
	FFVB1517 FLVB1517	40x40		52, 312, 32, 32	52, 312, 32, 32	52, 312, 40, 32			
	FFVA1760 FLVA1760	42.5x42.5		52, 676, 32, 16	52, 676, 32, 16	52, 676, 36, 16			
	FFVD1924 FLVD1924	45x45		52, 780, 28, 24	52, 780, 28, 24	52, 780, 28, 24	52, 780, 28, 24	52, 780, 28, 24	
	FFVE1924 FLVE1924	45x45		52, 624, 32, 32	52, 624, 32, 32	52, 624, 36, 36	52, 624, 36, 36	52, 624, 36, 36	
	FFVJ1924 FLVJ1924	45x45			52, 312, 32, 32	52, 312, 40, 40	52, 312, 52, 52	52, 312, 52, 52	
	FLVA2377	50x50				104, 936, 28, 24	52, 988, 28, 24	52, 988, 28, 24	
	FLVB2377	50x50							52, 1248, 36, 0
	FLVA2892	55x55							52, 1404, 48, 0

JESD204B References

ADI JESD204B Survival Guide

www.analog.com/static/imported-files/tech_articles/JESD204B-Survival-Guide.pdf

http://www.analog.com/static/imported-files/topic_pages/JESD204B-Transport-Layer.pdf

http://www.analog.com/static/imported-files/topic_pages/JESD204B-Data-Link-Layer.pdf

www.xilinx.com/products/technology/high-speed-serial/jesd204-high-speed-interface.html

Xilinx JESD204B White Paper

http://www.xilinx.com/support/documentation/white_papers/wp446-jesd204b.pdf

JESD204B References

JESD204B Link Latency Design Using a High Speed ADC and FPGA
http://www.ti.com/lit/ug/tidu171/tidu171.pdf

Xilinx References

www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug897-vivado-sysgen-user.pdf

http://www.xilinx.com/support/documentation/user_guides/ug576-ultrascale-gth-transceivers.pdf

Digital Signal Processing References

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Digital Receivers and Transmitters Using Polyphase Filter Banks for Wireless Communications

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CHANNELIZATION TECHNIQUES FOR SOFTWARE DEFINED RADIO

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http://www.spectrum-usa.com/channel_techniques/Channelization_Paper_SDR_forum.pdf