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Connector**
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GMII**
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XC6SLX16

U1

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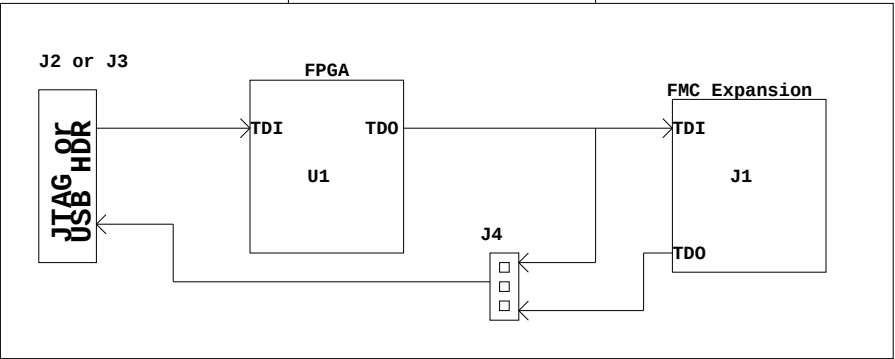
SPI X4 or
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IIC Addresssing

U5	0b1010100
J1	EEPROM: 0b1010010 Other Devices: 0bXXXXX10

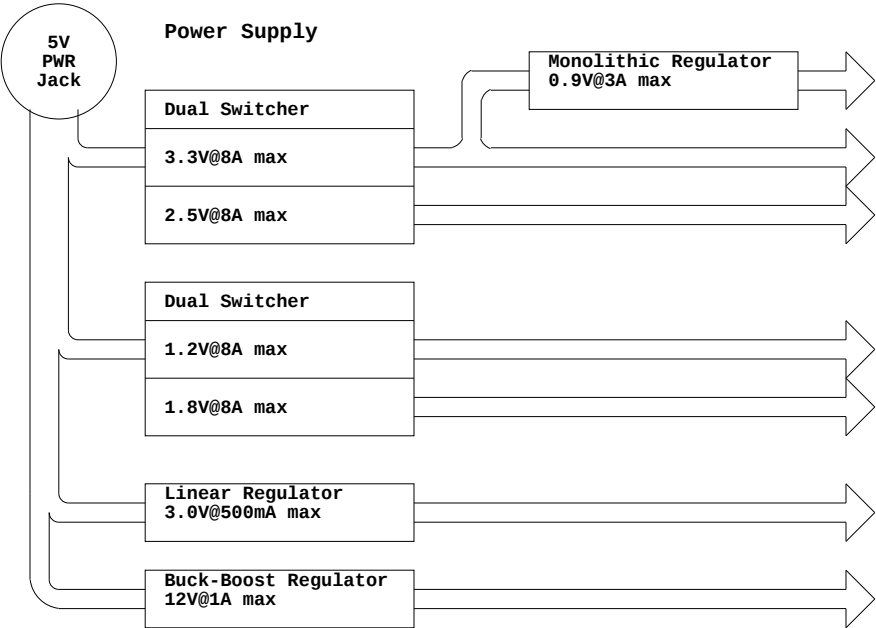
JTAG Chain



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Power Supply

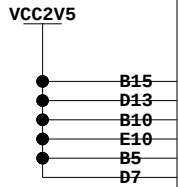


Title:	SP601 Block Diagram SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM	PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464
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Date:	10-20-2009_14:54	Ver:	C
Sheet Size:	B	Rev:	04
Sheet	1 of 16	Drawn By	BF

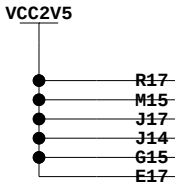
SOCKET
BANK 0
sa16cs324

IO_L30N_0_SCP0_A16	A16	FMC_LA04_N	6
IO_L30P_0_SCP1_B16	B16	FMC_LA04_P	6
IO_L29N_0_SCP2_C14	C14	GPIO_LED_1	9
IO_L29P_0_SCP3_D14	D14	GPIO_SWITCH_0	9
IO_L28N_0_SCP4_A15	A15	FMC_LA02_N	6
IO_L28P_0_SCP5_C15	C15	FMC_LA02_P	6
IO_L27N_0_SCP6_E13	E13	GPIO_LED_0	9
IO_L27P_0_SCP7_F13	F13	GPIO_HDR6	10
IO_L26N_0_VREF_0_A14	A14	FMC_LA05_N	6
IO_L26P_0_B14	B14	FMC_LA05_P	6
IO_L25N_0_E12	E12	GPIO_SWITCH_1	9
IO_L25P_0_F12	F12	GPIO_SWITCH_2	9
IO_L24N_0_A13	A13	FMC_LA03_N	6
IO_L24P_0_C13	C13	FMC_LA03_P	6
IO_L23N_0_C12	C12	FMC_LA06_N	6
IO_L23P_0_D12	D12	FMC_LA06_P	6
IO_L22N_0_E11	E11	FMC_LA08_N	6
IO_L22P_0_F11	F11	FMC_LA08_P	6
IO_L21N_0_A12	A12	FMC_LA11_N	6
IO_L21P_0_B12	B12	FMC_LA11_P	6
IO_L20N_0_F10	F10	FMC_LA09_N	6
IO_L20P_0_G11	G11	FMC_LA09_P	6
IO_L19N_0_A11	A11	FMC_LA13_N	6
IO_L19P_0_B11	B11	FMC_LA13_P	6
IO_L18N_0_VREF_0_F9	F9	FMC_LA15_N	6
IO_L18P_0_G9	G9	FMC_LA15_P	6
IO_L17N_0_GCLK12_A10	A10	FMC_CLK0_M2C_N	6
IO_L17P_0_GCLK13_C10	C10	FMC_CLK0_M2C_P	6
IO_L16N_0_GCLK14_C11	C11	FMC_LA01_CC_N	6
IO_L16P_0_GCLK15_D11	D11	FMC_LA01_CC_P	6
IO_L15N_0_GCLK16_A9	A9	PHY_TXCLK	7
IO_L15P_0_GCLK17_B9	B9	PHY_TXCLK	7
IO_L14N_0_GCLK18_C9	C9	FMC_LA00_CC_N	6
IO_L14P_0_GCLK19_D9	D9	FMC_LA00_CC_P	6
IO_L13N_0_A8	A8	PHY_TXER	7
IO_L13P_0_B8	B8	PHY_TXCTL_TXEN	7
IO_L12N_0_F8	F8	PHY_TXD0	7
IO_L12P_0_G8	G8	PHY_TXD1	7
IO_L11N_0_C8	C8	FMC_LA10_N	6
IO_L11P_0_D8	D8	FMC_LA10_P	6
IO_L10N_0_A7	A7	FMC_LA16_N	6
IO_L10P_0_C7	C7	FMC_LA16_P	6
IO_L09N_0_E8	E8	FMC_LA07_N	6
IO_L09P_0_F7	F7	FMC_LA07_P	6
IO_L08N_0_VREF_0_A6	A6	PHY_TXD2	7
IO_L08P_0_B6	B6	PHY_TXD3	7
IO_L07N_0_E6	E6	PHY_TXD4	7
IO_L07P_0_F7	F7	PHY_TXD5	7
IO_L06N_0_A5	A5	PHY_TXD6	7
IO_L06P_0_C5	C5	PHY_TXD7	7
IO_L05N_0_A4	A4	GPIO_LED_3	9
IO_L05P_0_B4	B4	GPIO_HDR5	10
IO_L04N_0_A3	A3	GPIO_HDR2	10
IO_L04P_0_B3	B3	FMC_PWR_GOOD_FLASH_RST	6, 8
IO_L03N_0_C6	C6	FMC_LA12_N	6
IO_L03P_0_D6	D6	FMC_LA12_P	6
IO_L02N_0_A2	A2	FMC_LA14_N	6
IO_L02P_0_B2	B2	FMC_LA14_P	6
IO_L01N_0_VREF_0_C4	C4	GPIO_LED_2	9
IO_L01P_0_HSWAPEN_D4	D4	FPGA_HSWAPEN	6

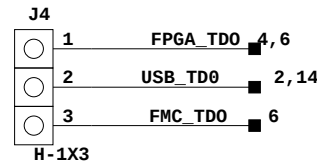


SOCKET
BANK 1
sa16cs324

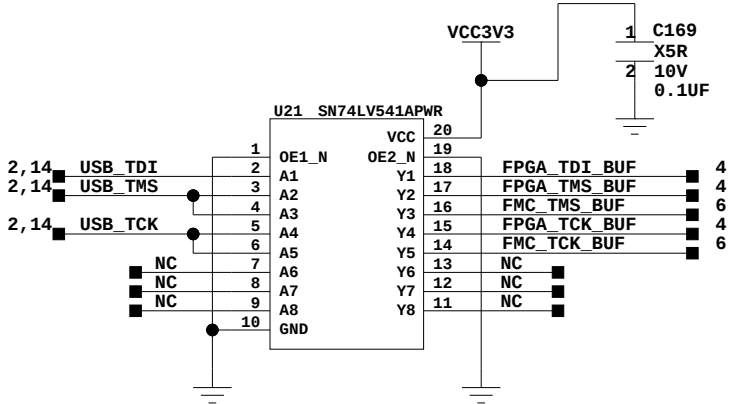
IO_L28N_1_DOUT_P16	P16	PHY_MDIO	7
IO_L28P_1_AWAKE_P15	P15	FPGA_AWAKE	8
IO_L27N_1_M13	M13	PHY_CRS	7
IO_L27P_1_L14	L14	PHY_COL	7
IO_L26N_1_VREF_1_N14	N14	PHY_MDC	7
IO_L26P_1_M14	M14	PHY_RXD0	7
IO_L25N_1_M1DQ15_U18	U18	PHY_RXD1	7
IO_L25P_1_M1DQ14_U17	U17	PHY_RXD2	7
IO_L24N_1_M1DQ13_T18	T18	PHY_RXD3	7
IO_L24P_1_M1DQ12_T17	T17	PHY_RXD4	7
IO_L23N_1_M1UDQSN_N16	N16	PHY_RXD5	7
IO_L23P_1_M1UDQS_N15	N15	PHY_RXD6	7
IO_L22N_1_M1DQ11_P18	P18	PHY_RXD7	7
IO_L22P_1_M1DQ10_P17	P17	PHY_RXER	7
IO_L21N_1_M1DQ9_N18	N18	PHY_RXCTL_RXDV	7
IO_L21P_1_HDC_M1DQ8_N17	N17	GPIO_HDR0	10
IO_L20N_1_LDC_M1DQ1_M18	M18	GPIO_HDR1	10
IO_L20P_1_FWE_B_M1DQ0_M16	M16	FLASH_WE_B	8
IO_L19N_1_FOE_B_M1DQ3_L18	L18	FLASH_OE_B	8
IO_L19P_1_FCS_B_M1DQ2_L17	L17	FLASH_CE_B	8
IO_L18N_1_A0_M1LDQSN_K18	K18	FLASH_A0	8
IO_L18P_1_A1_M1LDQS_K17	K17	FLASH_A1	8
IO_L17N_1_A2_M1DQ7_J18	J18	FLASH_A2	8
IO_L17P_1_A3_M1DQ6_J16	J16	FLASH_A3	8
IO_L16N_1_GCLK4_M1DQ5_H18	H18	SMACLK_N	9
IO_L16P_1_GCLK5_M1DQ4_H17	H17	SMACLK_P	9
IO_L15N_1_GCLK6_TRDY1_M1LDM_L16	L16	PHY_RXCLK	7
IO_L15P_1_GCLK7_M1UDM_L15	L15	GPIO_HDR3	10
IO_L14N_1_GCLK8_M1CASN_K16	K16	SYSCLK_N	9
IO_L14P_1_GCLK9_IRDY1_M1RASNK15	K15	SYSCLK_P	9
IO_L13N_1_GCLK10_M1A6_L13	L13	PHY_RESET	7
IO_L13P_1_GCLK11_M1A5_L12	L12	USB_1_RX	10
IO_L12N_1_M10DT_K14	K14	USB_1_TX	10
IO_L12P_1_M1A3_J13	J13	PHY_INT	7
IO_L11N_1_A4_M1CLKN_G18	G18	FLASH_A4	8
IO_L11P_1_A5_M1CLK_G16	G16	FLASH_A5	8
IO_L10N_1_A6_M1A1_H16	H16	FLASH_A6	8
IO_L10P_1_A7_M1A0_H15	H15	FLASH_A7	8
IO_L09N_1_A8_M1BA1_H14	H14	FLASH_A8	8
IO_L09P_1_A9_M1BA0_H13	H13	FLASH_A9	8
IO_L08N_1_A10_M1A2_F18	F18	FLASH_A10	8
IO_L08P_1_A11_M1A7_F17	F17	FLASH_A11	8
IO_L07N_1_A12_M1BA2_K13	K13	FLASH_A12	8
IO_L07P_1_A13_M1WE_K12	K12	FLASH_A13	8
IO_L06N_1_A14_M1A4_E18	E18	FLASH_A14	8
IO_L06P_1_A15_M1A10_E16	E16	FLASH_A15	8
IO_L05N_1_A16_M1A9_G13	G13	FLASH_A16	8
IO_L05P_1_A17_M1A8_H12	H12	FLASH_A17	8
IO_L04N_1_A18_M1A12_D18	D18	FLASH_A18	8
IO_L04P_1_A19_M1CKE_D17	D17	FLASH_A19	8
IO_L03N_1_A20_M1A11_G14	G14	FLASH_A20	8
IO_L03P_1_A21_M1RESET_F14	F14	FLASH_A21	8
IO_L02N_1_A22_M1A14_C18	C18	FLASH_A22	8
IO_L02P_1_A23_M1A13_C17	C17	FLASH_A23	8
IO_L01N_1_A24_VREF_1_F16	F16	FLASH_A24	8
IO_L01P_1_A25_F15	F15	GPIO_HDR4	10



U1

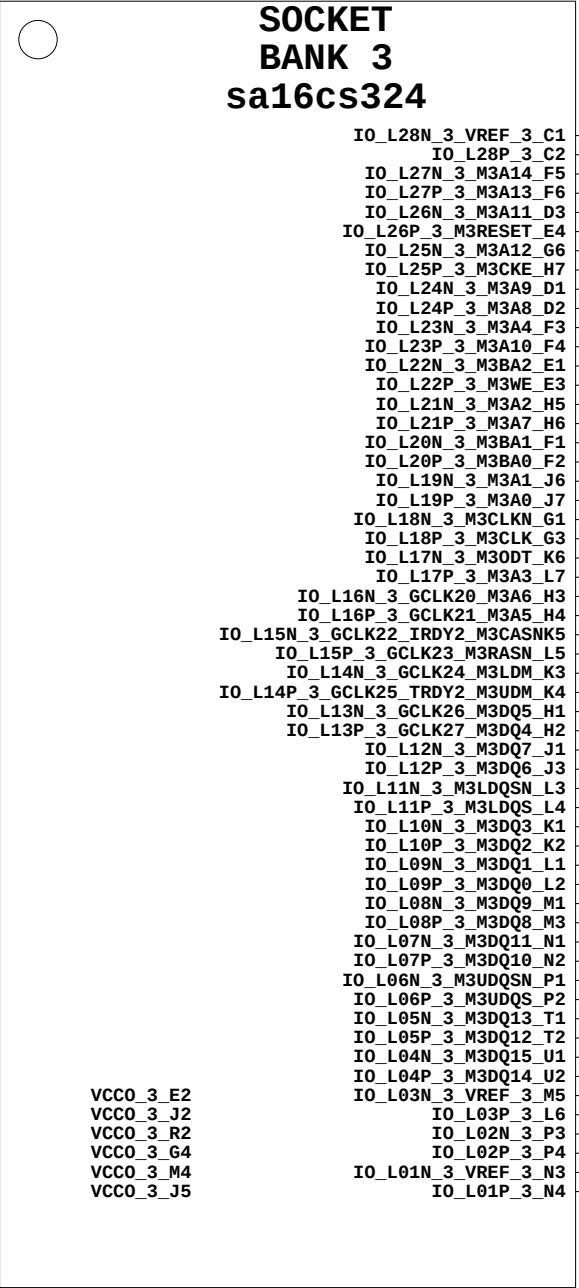
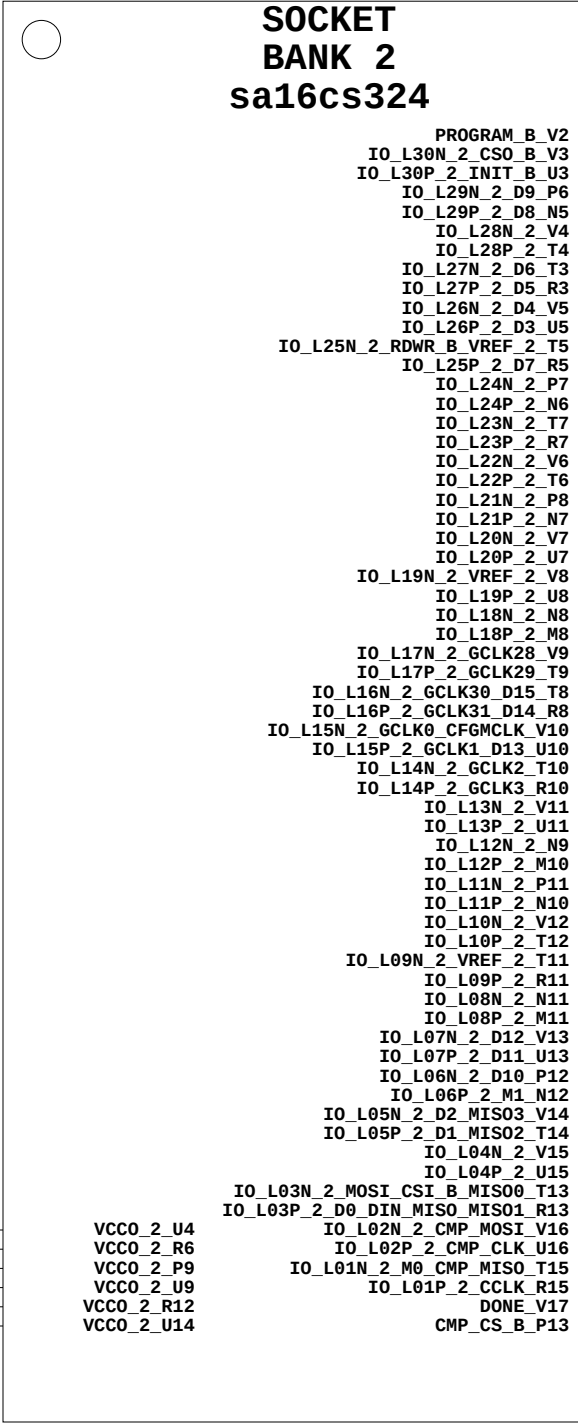


Jumper to include FMC
in JTAG chain



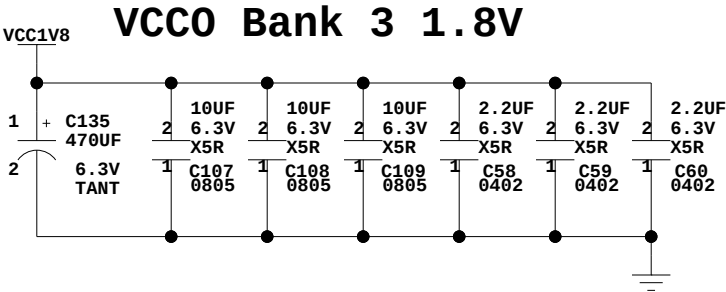
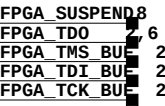
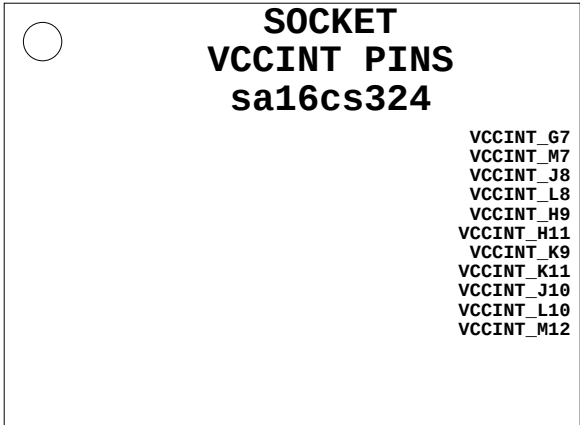
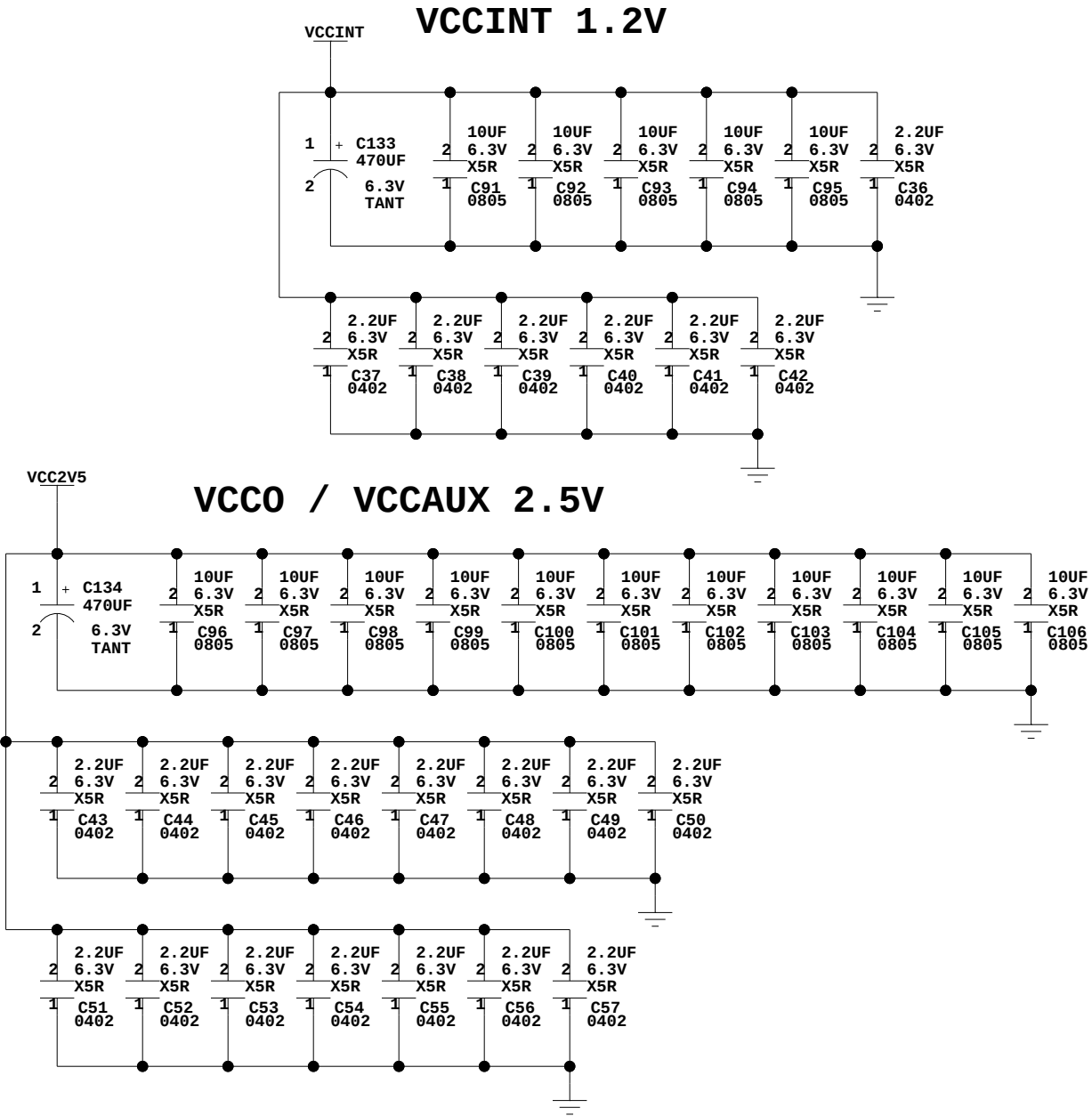
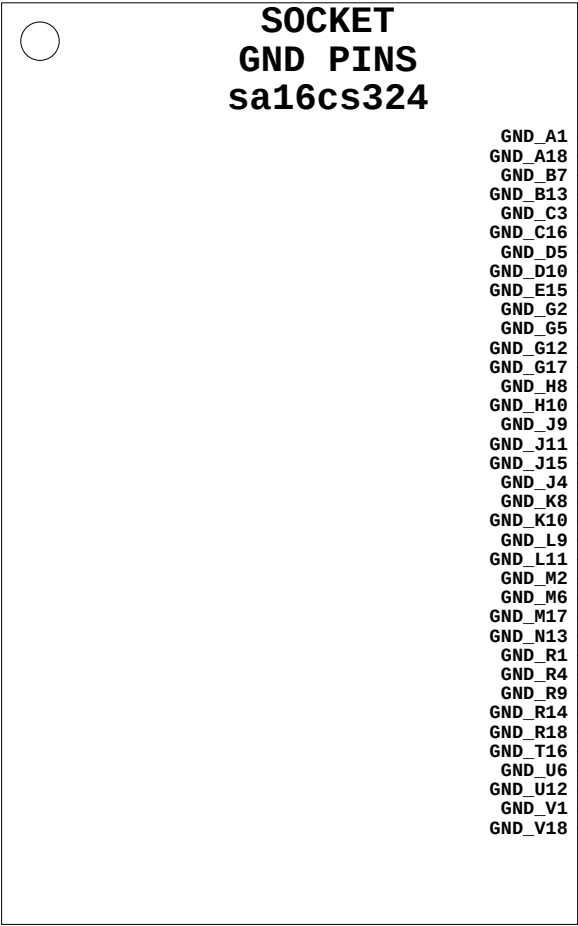
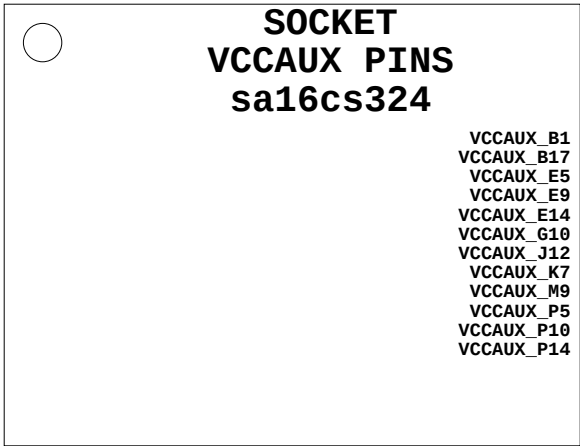
Banks 0, 1

Title:	Banks 0, 1 SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM	PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464
Date:	10-20-2009_14:56	Ver: C
Sheet Size:	B	Rev: 04
Sheet	2 of 16	Drawn By BF



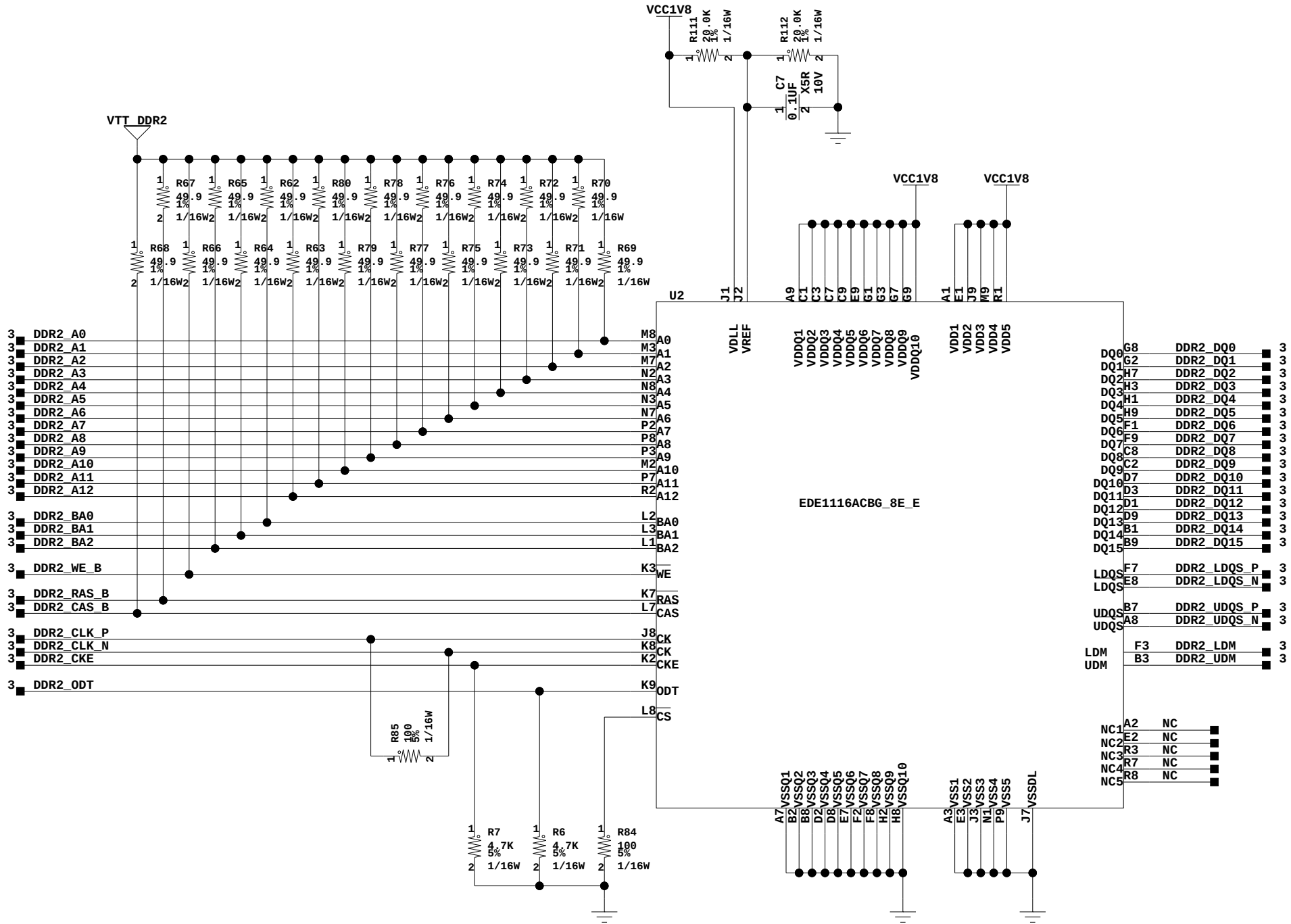
Banks 2, 3

			
Title: Banks 2, 3 SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date: 10-20-2009_14:56		Ver: C	
Sheet Size: B		Rev: 04	
Sheet 3 of 16		Drawn By BF	

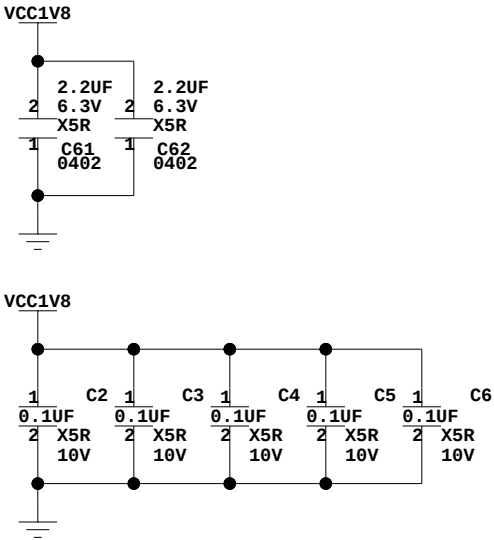


GND Bank, Decoupling caps

			
Title: GND Bank, Decoupling caps SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date: 10-20-2009_14:54		Ver: C	
Sheet Size: B		Rev: 04	
Sheet 4 of 16		Drawn By BF	

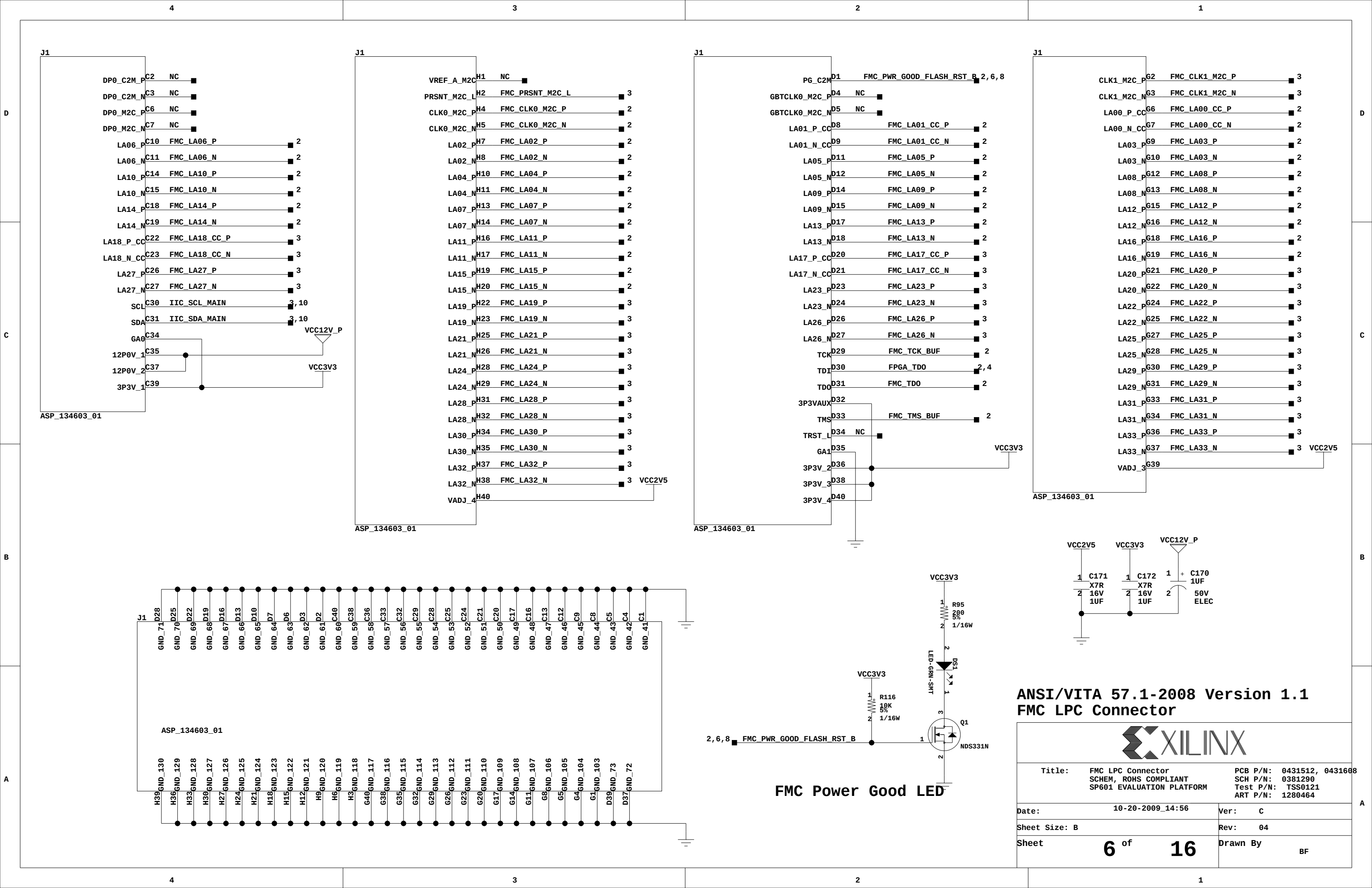


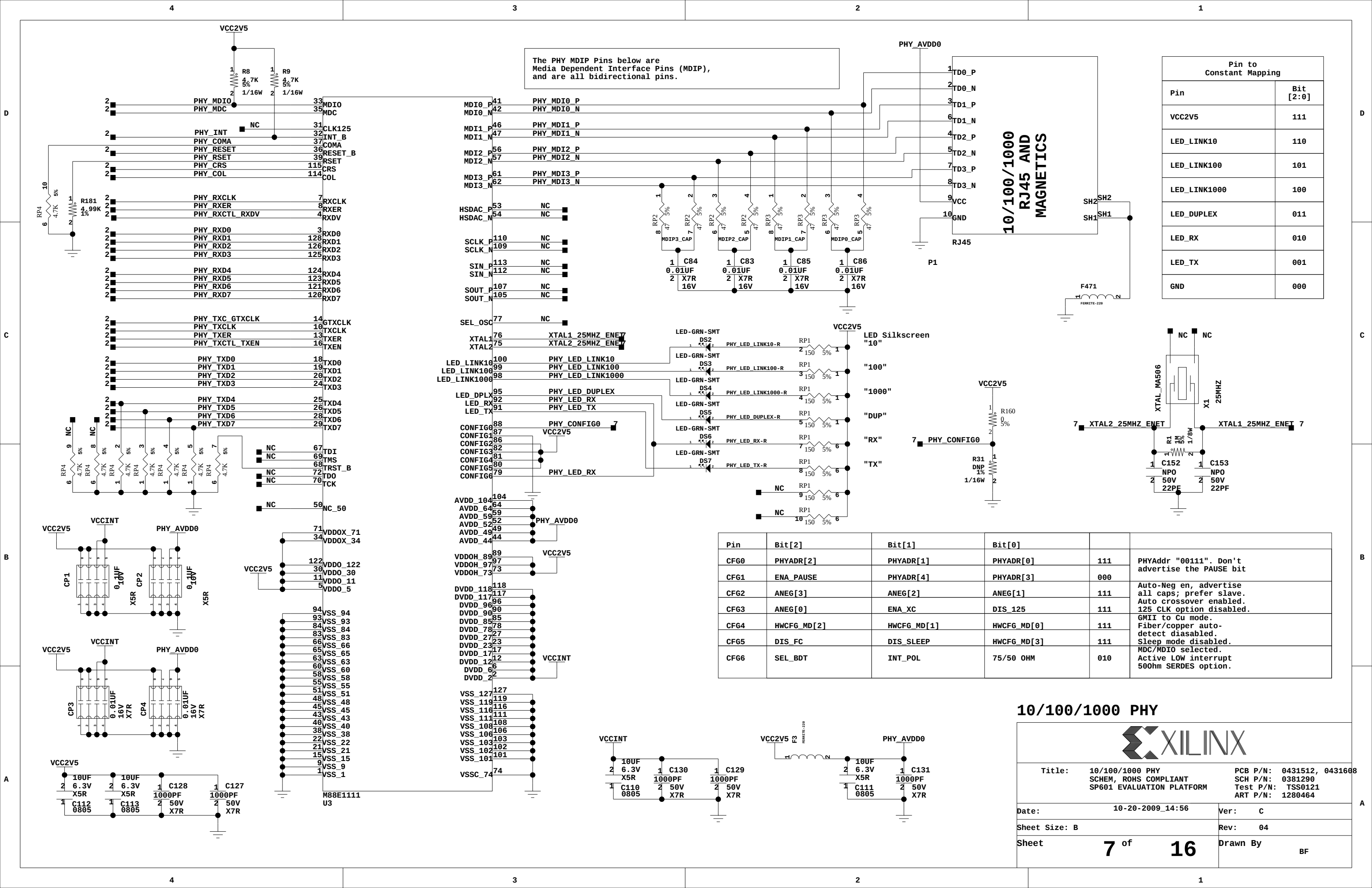
DDR2 Decoupling

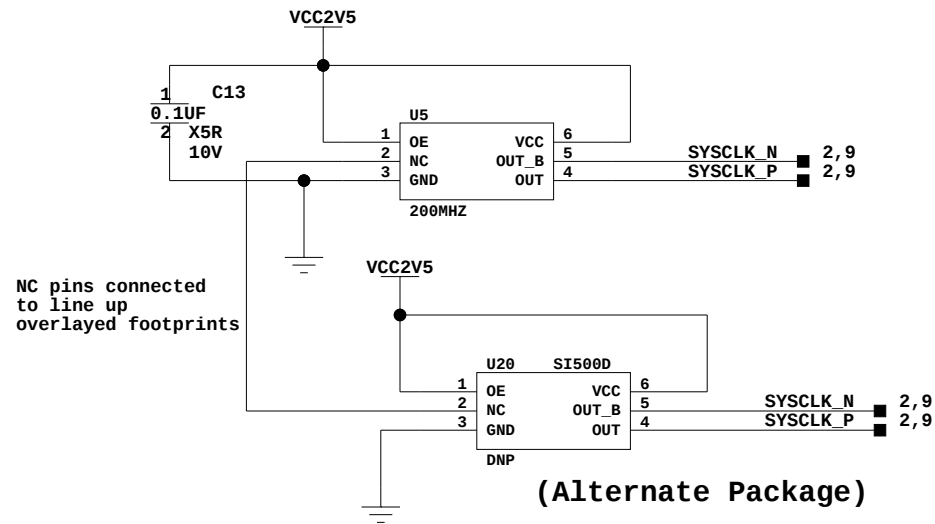


DDR2 SDRAM

Title: DDR2 SDRAM SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date:	10-20-2009_14:56	Ver:	C
Sheet Size:	B	Rev:	04
Sheet	5 of 16	Drawn By	BF

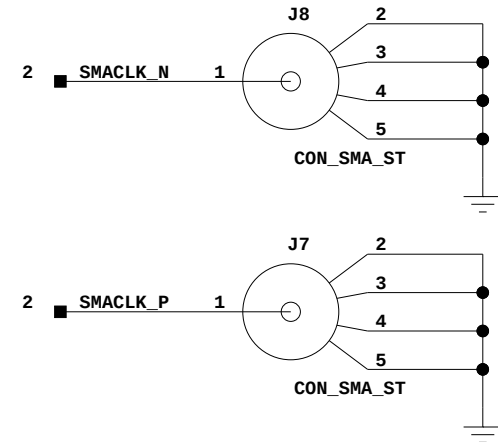




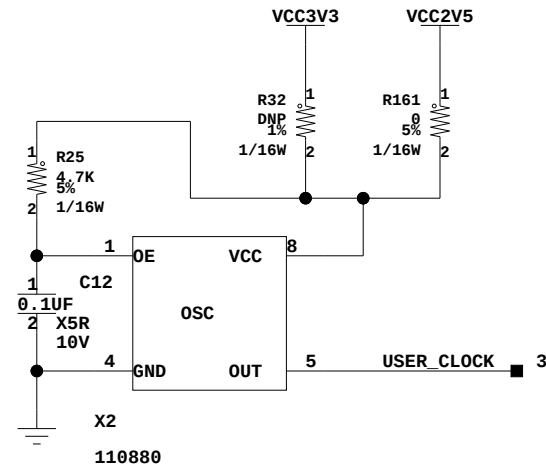


(Alternate Package)

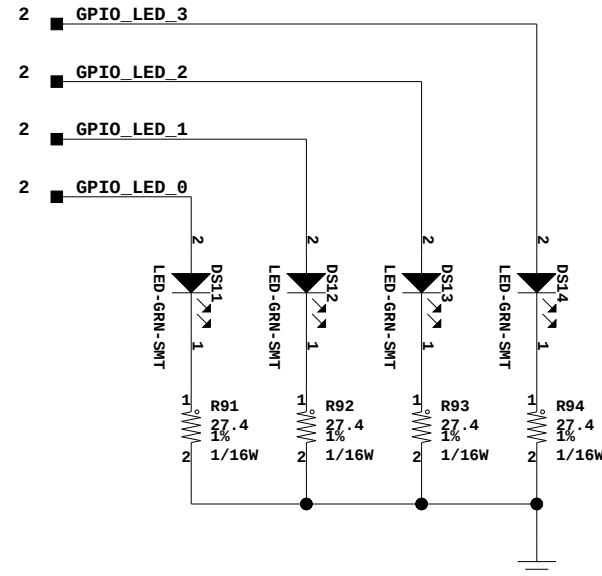
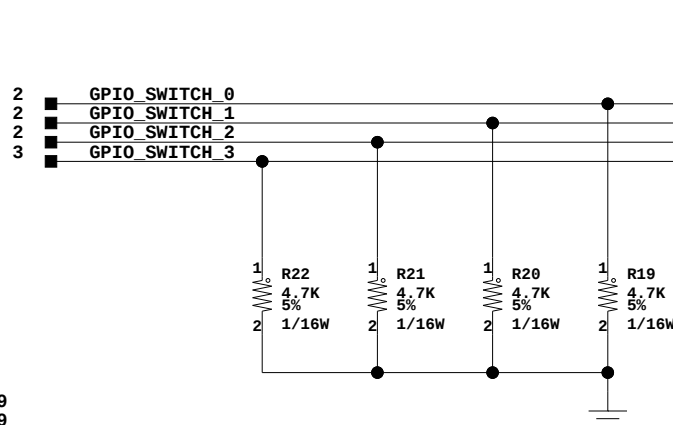
Differential System Clock



SMA Differential Clock

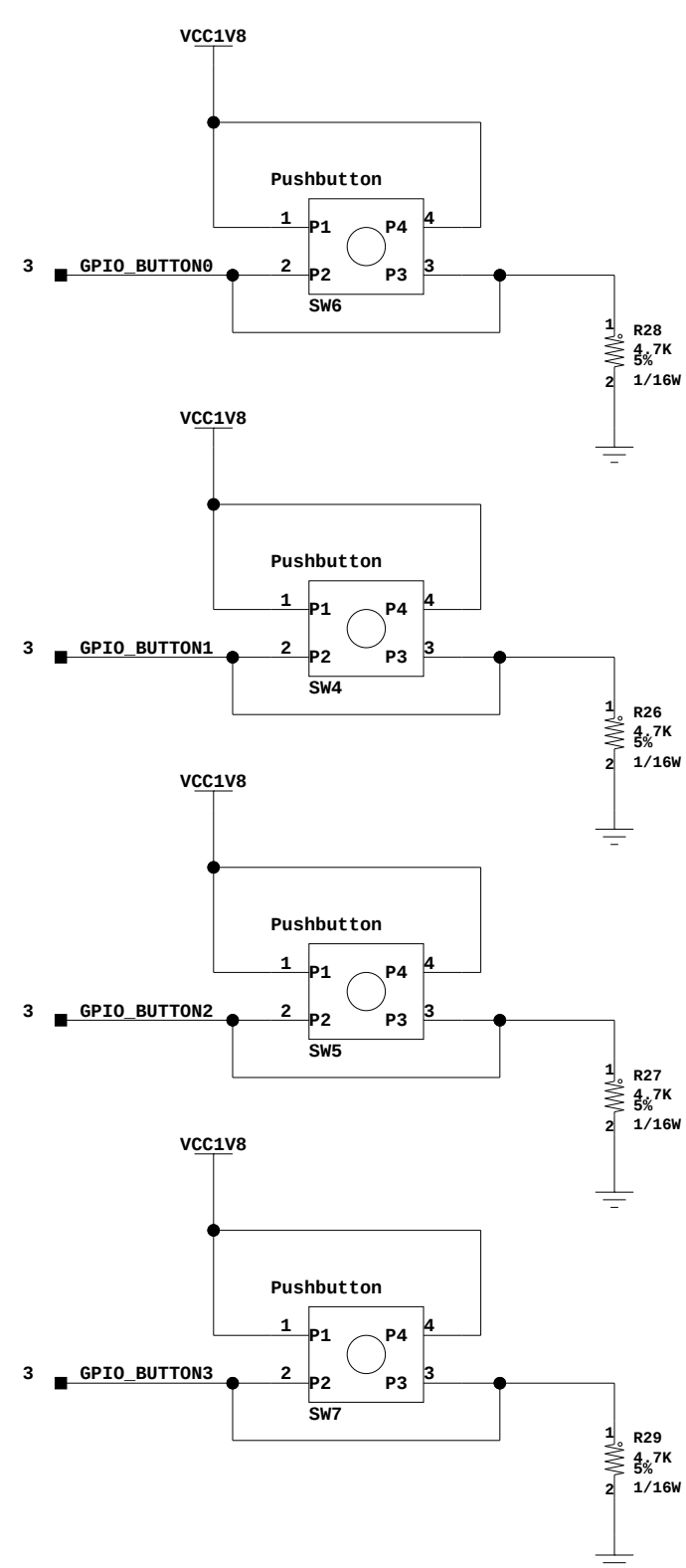
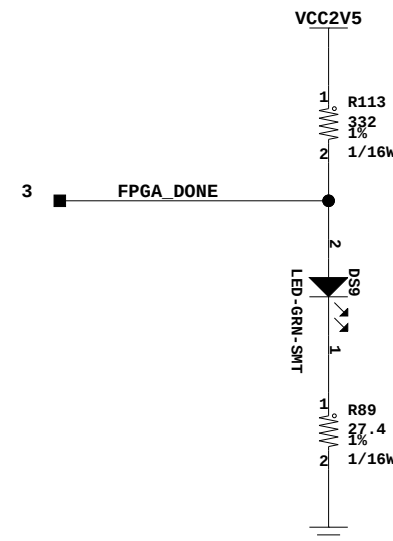
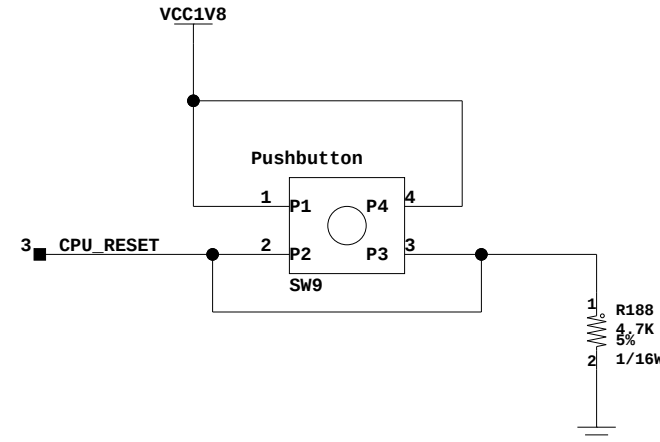
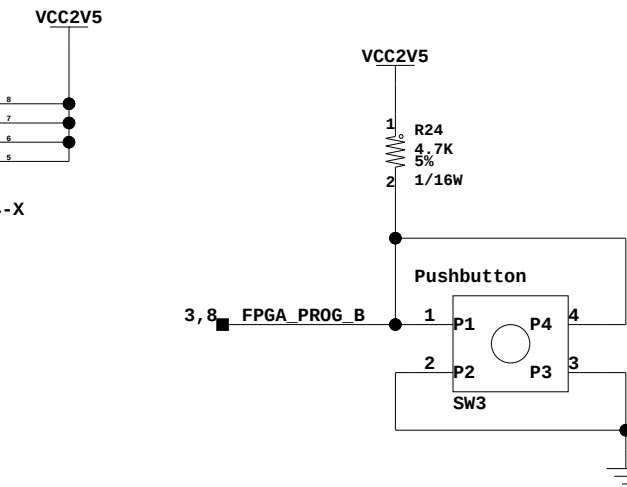


Single Ended User Clock



INIT_B = 0, LED: ON
INIT_B = 1, LED: OFF

FPGA_INIT_B

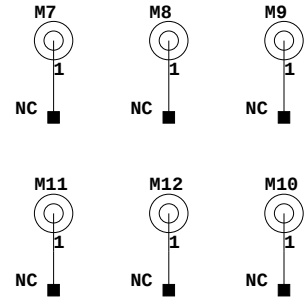
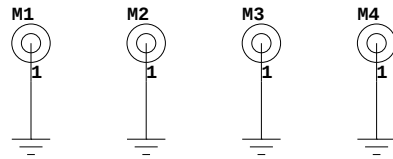
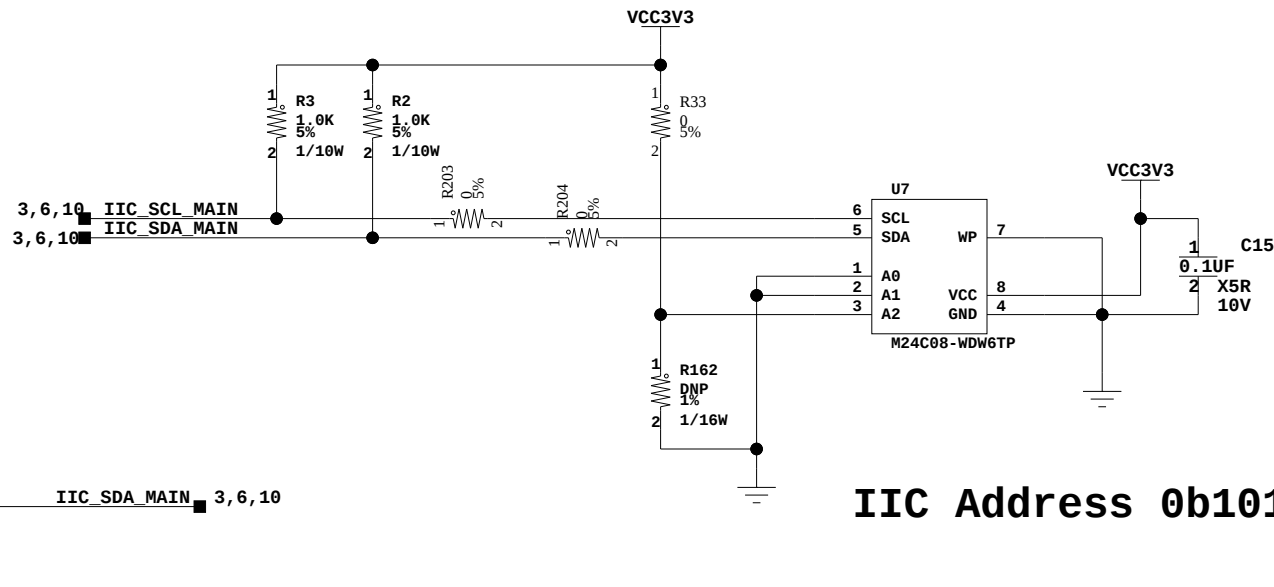


Clocks, LEDs, Buttons, Switches



Title: Clocks, LEDs, Buttons, SwitchesPCB P/N: 0431512, 0431608
SCHEM, ROHS COMPLIANT SCH P/N: 0381290
SP601 EVALUATION PLATFORM Test P/N: TSS0121
ART P/N: 1280464

Date: 3-17-2010_8:42 Ver: C
Sheet Size: B Rev: 04
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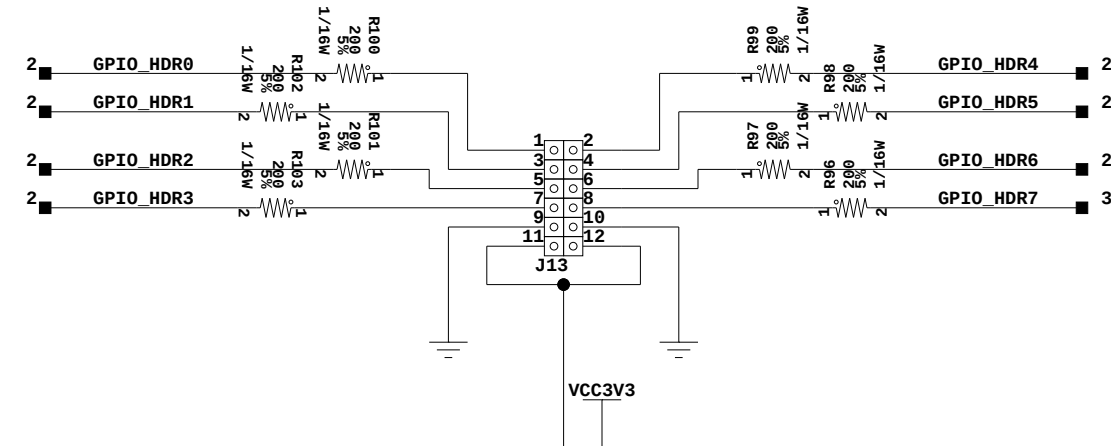
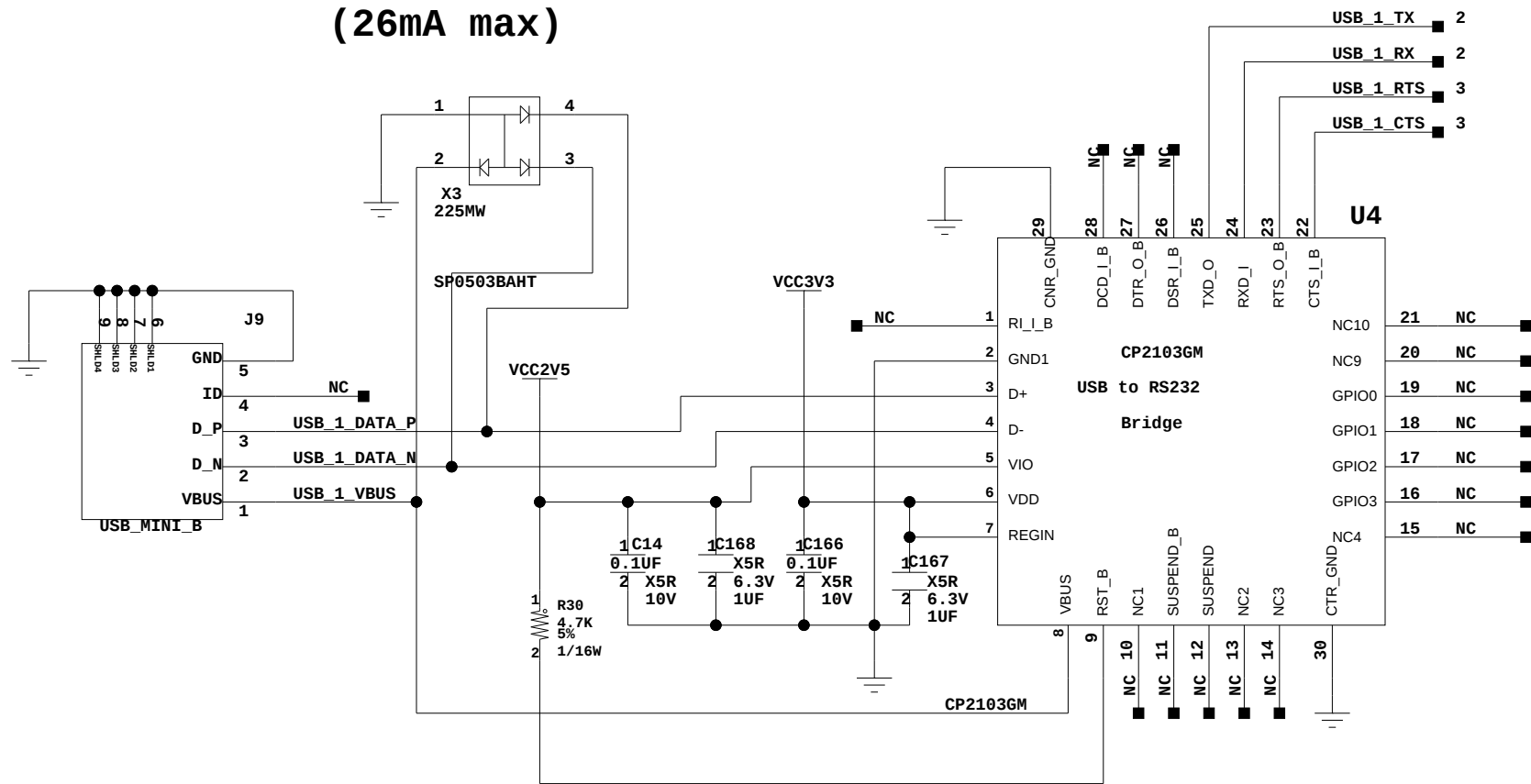


Mounting Holes

Fiducials

IIC Address 0b1010100

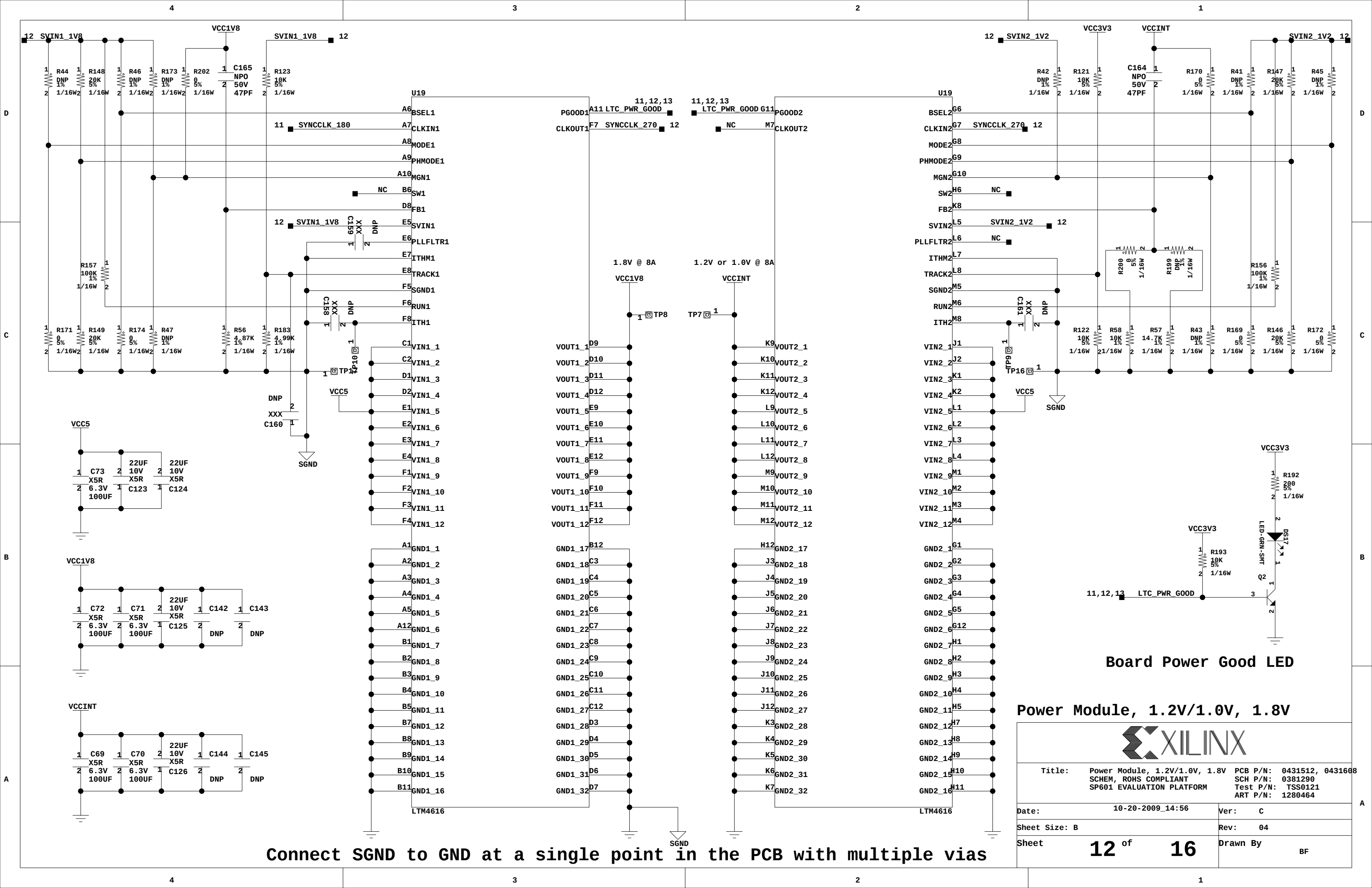
CP2103 USB Self-Powered
(26mA max)

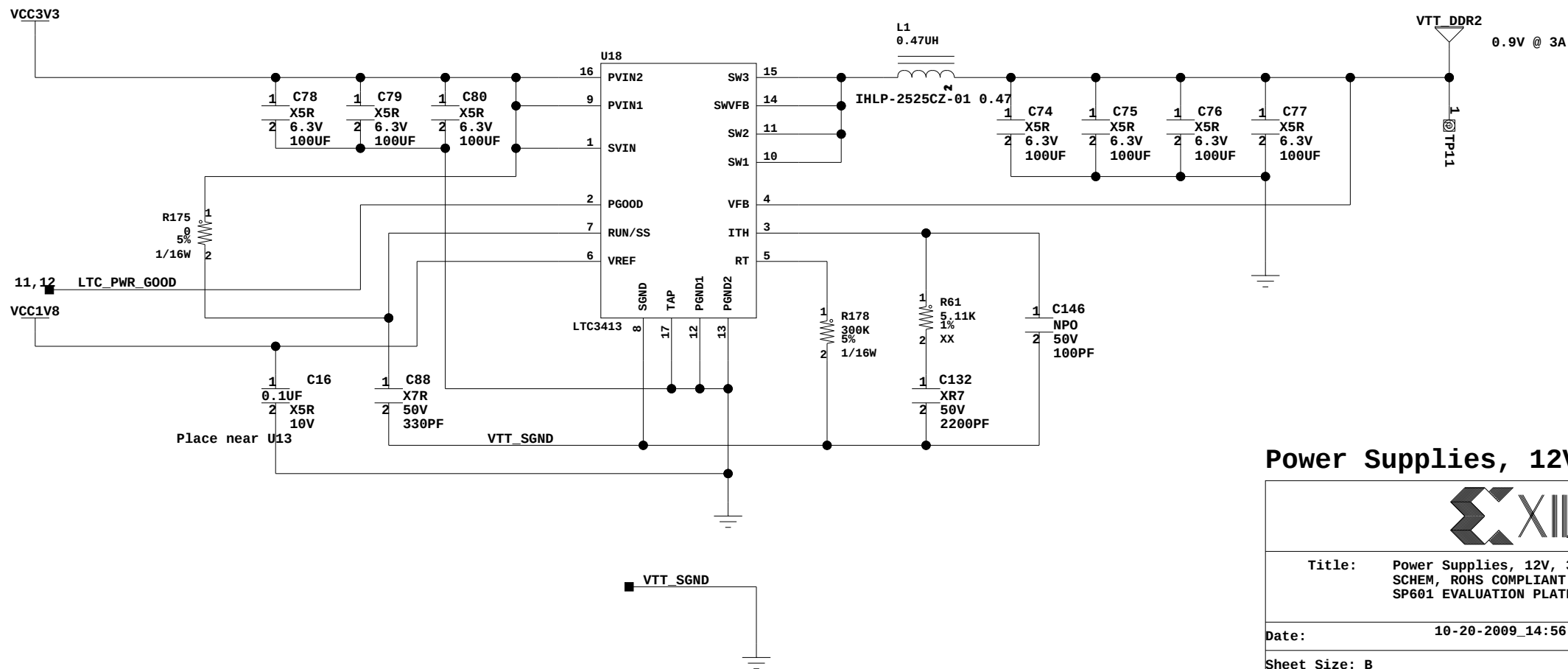
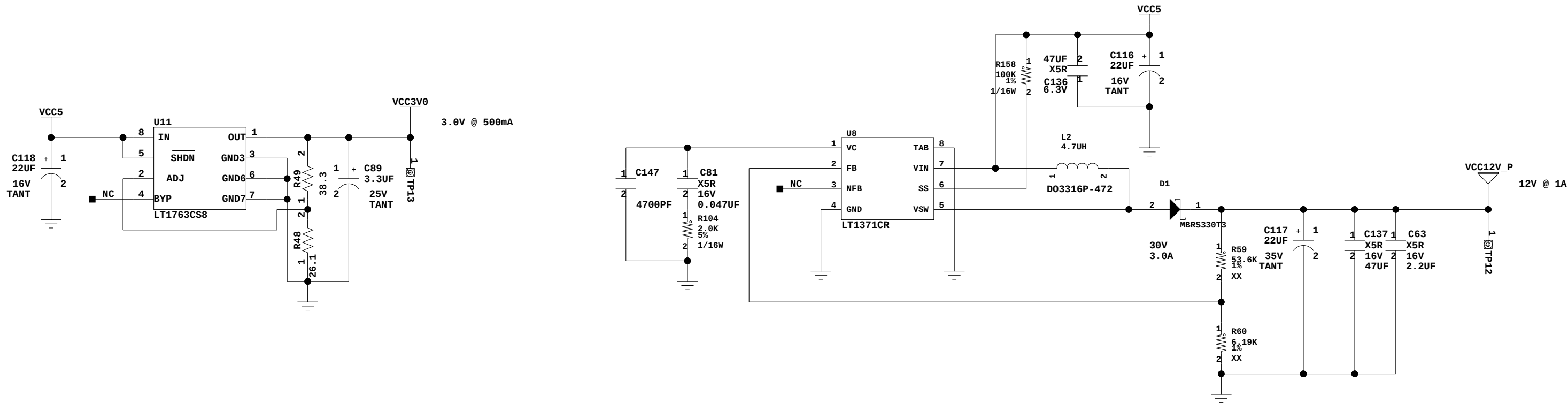


The VIO voltage must match the appropriate bank IO voltage

UART, IIC Header/EEPROM, GPIO Headers

Title: UART, IIC Header/EEPROM, GPIO Headers SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date: 10-20-2009_14:56		Ver: C	
Sheet Size: B		Rev: 04	
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Power Supplies, 12V, 3.0V, 0.9V



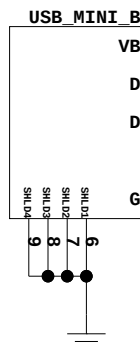
Title: Power Supplies, 12V, 3.0V, 0.9VPCB P/N: 0431512, 0431608
SCHEM, ROHS COMPLIANT SCH P/N: 0381290
SP601 EVALUATION PLATFORM Test P/N: TSS0121
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Date: 10-20-2009_14:56 Ver: C
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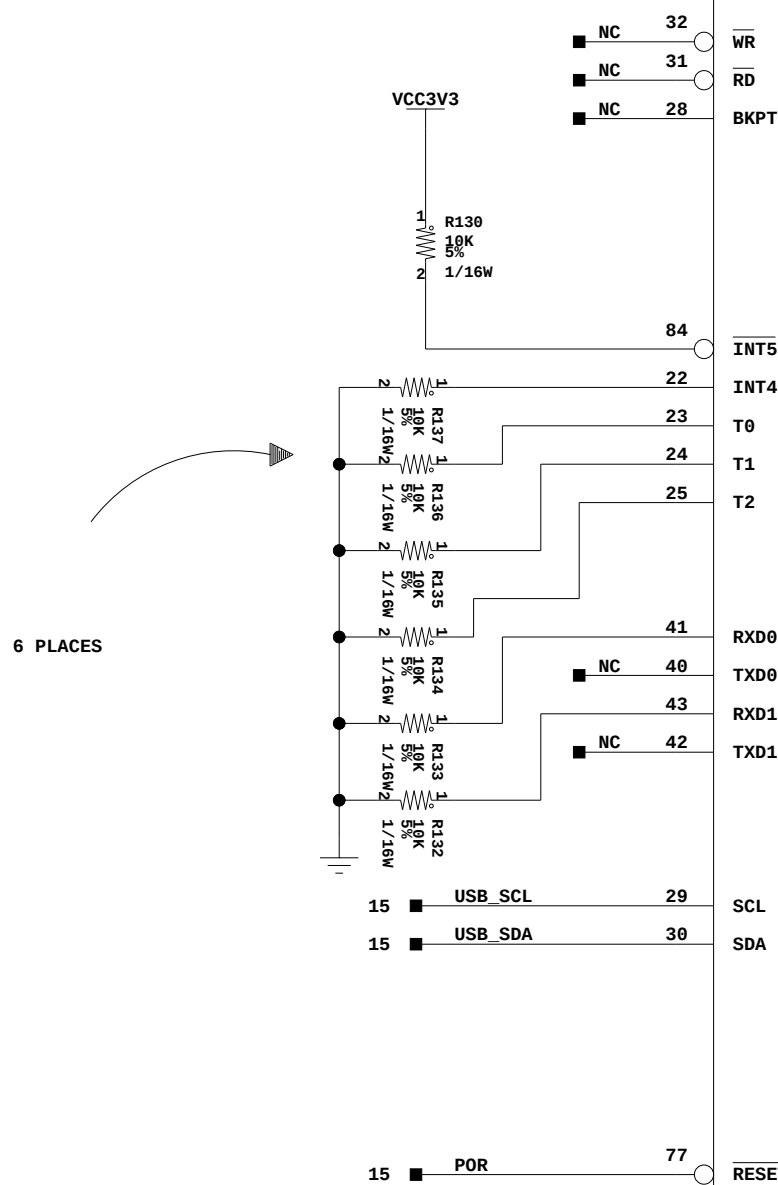
The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

USB CONNECTOR

USB TYPE B RECEPTACLE



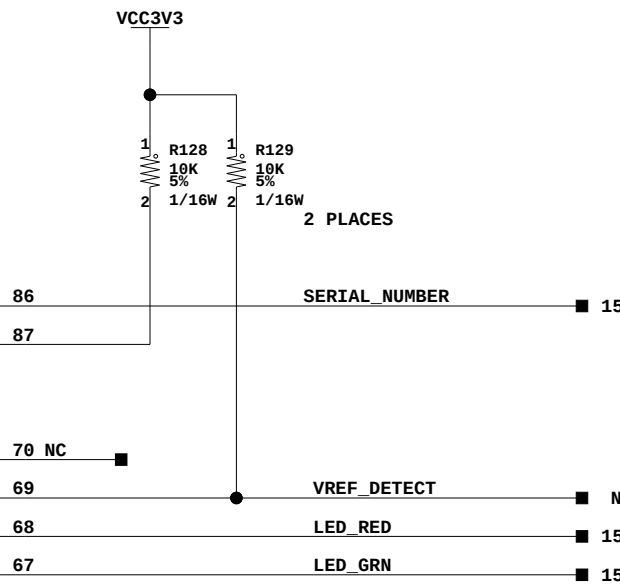
NOTE: EMBEDDED VERSION IS NOT BUS POWERED



PART_NUMBER=CY7C68013A

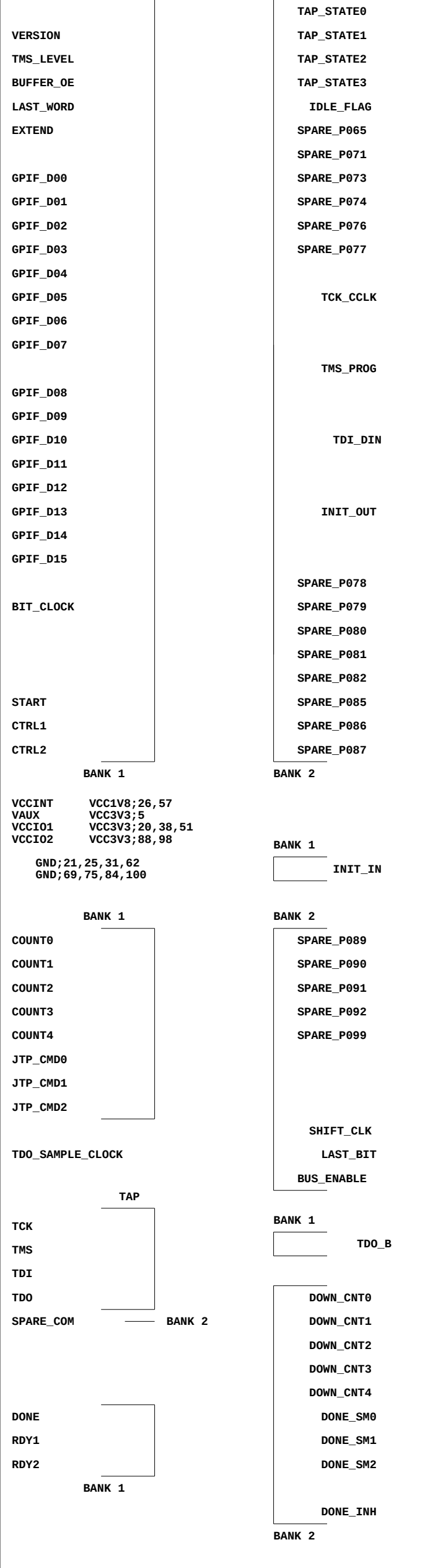
USB CONTROLLER

VCCINT VCC3V3;1,16,20,33,38
VCC3V3;49,53,66,78,85
GND;65,75,94,99
GND;2,19,21,39,48,50



U9

PART_NUMBER=XC2C256



PARALLEL TO SERIAL CONVERTER

NOTE:

MAKE PARALLEL CONNECTIONS TO J1 (OPTION B) AT EACH OF THE NETS MARKED (B) TO FACILITATE FASTER IN-CIRCUIT RE-PROGRAMMING OF THE CPLD DURING BOARD TEST. J1 DOES NOT NEED TO BE POPULATED DURING PRODUCTION, BUT THE ASSEMBLY FOOTPRINT IS RECOMMENDED FOR THE PWB LAYOUT.

TARGET INTERFACE CONNECTIONS	
FROM	TO JTAG
FPGA_TCK	TCK ALL DEVICES
FPGA_TMS	TMS ALL DEVICES
USB_HEADER_TDI	FIRST DEVICE TDI
JTAG_TDO	LAST DEVICE TDO
EMBEDDED_INIT	NO CONNECTION

3.3V INTERFACE TO LOCAL JTAG OR SLAVE-SERIAL DEVICE CHAIN.
FOR LONG CHAINS OR TRACES, DISTRIBUTE EMBEDDED_TCK AND EMBEDDED_TMS WITH LVDS BUFFERS.

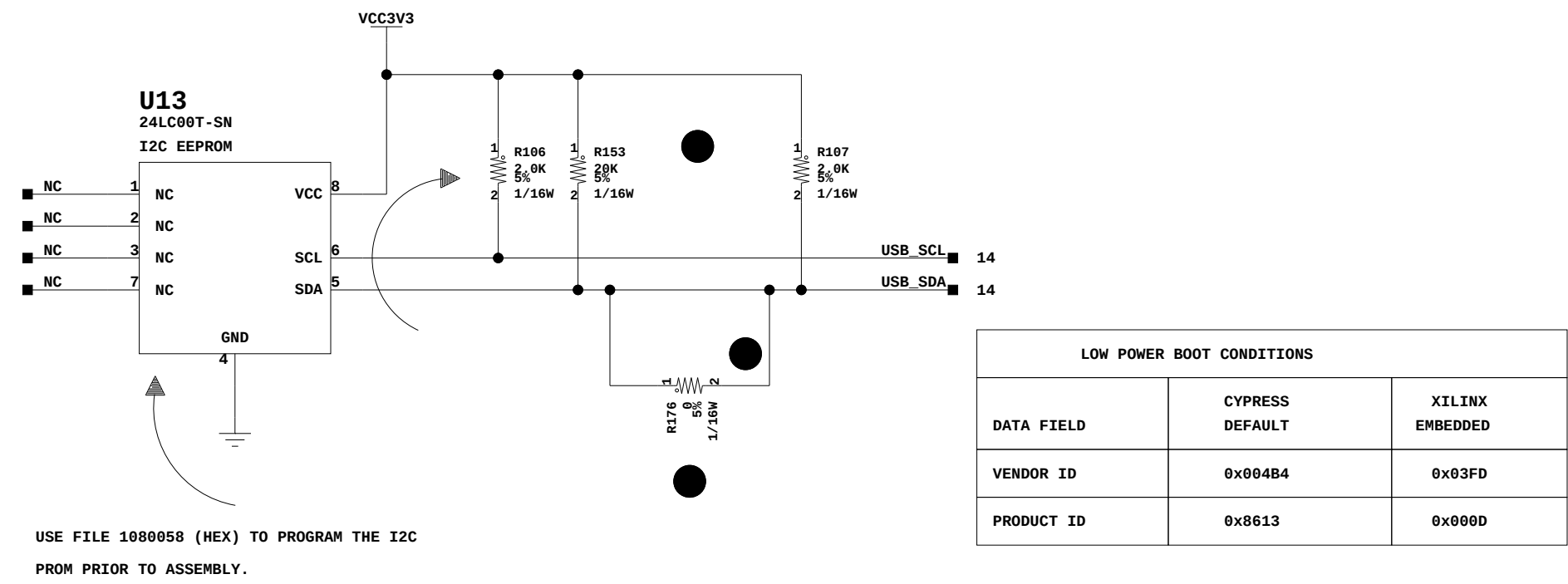
LEGEND:

- (B) OPTIONAL NETS ROUTED IN PARALLEL TO LOCAL 2MM CABEL CONNECTOR J1.
- COMPONENTS TO BE LOADED FOR THE PRODUCTION ASSEMBLY VERSION ONLY.
- OPTIONAL COMPONENTS THAT SUPPORT DEBUG AND/OR DIAGNOSTICS.

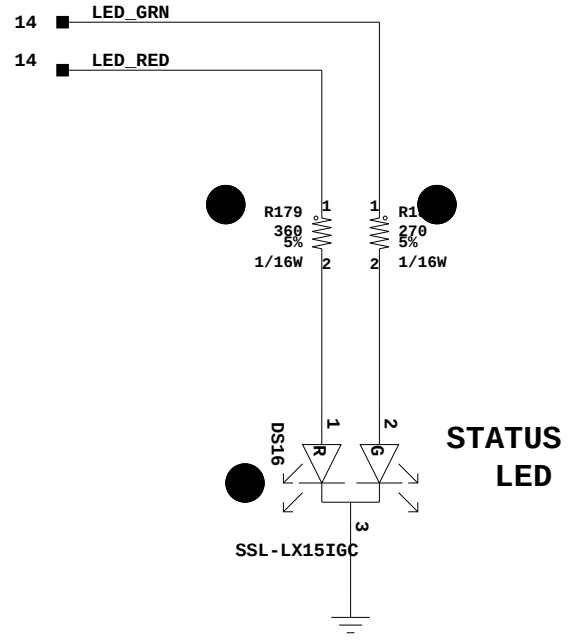
Embedded USB JTAG: USB Controller, CPLD

The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

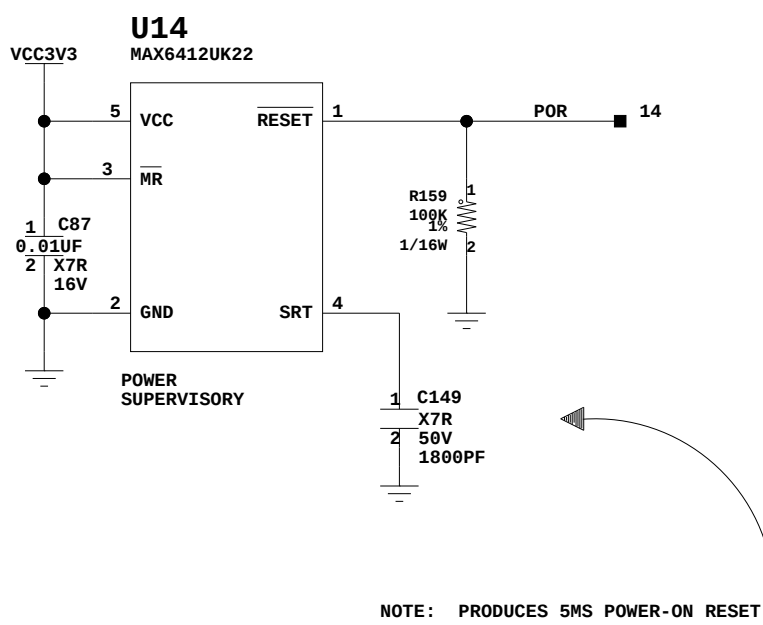
DEFAULT PID/VID EEPROM



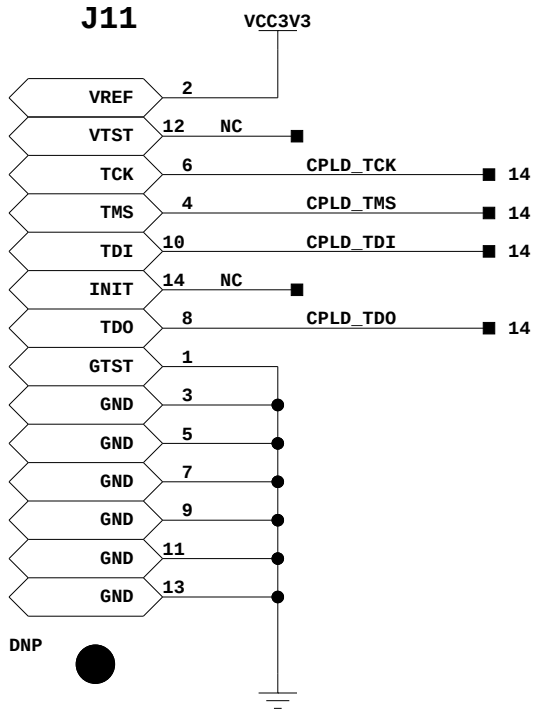
STATUS LEDS (OPTION A)



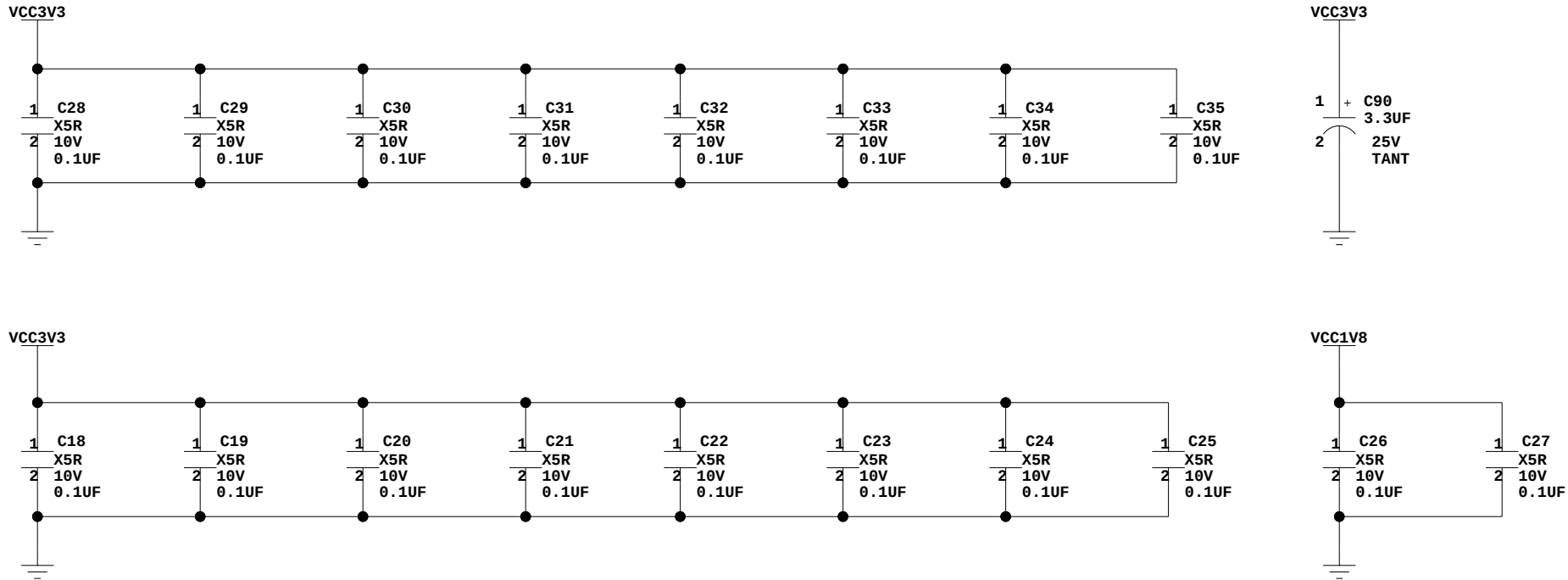
POWER-ON RESET



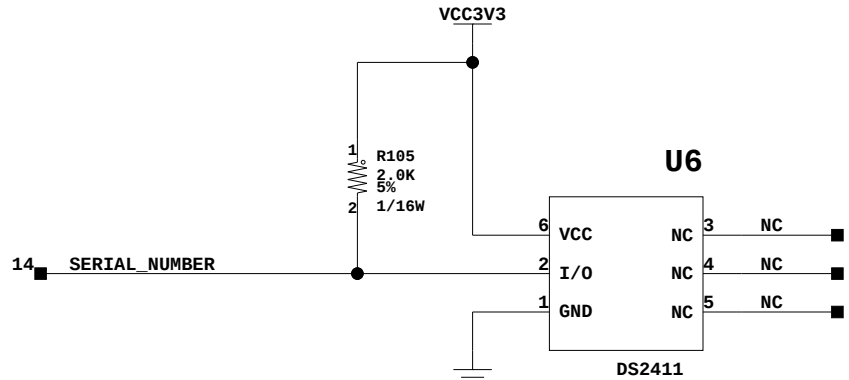
PC4 JTAG CONNECTOR (OPTION B)



BYPASS CAPACITORS



ELECTRONIC SERIAL NUMBER



Embedded USB JTAG: IIC, POR, Decoupling, LED, JTAG Header, Serial Number



MACHINE_SCREW_SS_PHILHD_4-40_X_3-8



MACHINE_SCREW_SS_PHILHD_4-40_X_3-8



MACHINE_SCREW_SS_PHILHD_4-40_X_3-8



MACHINE_SCREW_SS_PHILHD_4-40_X_3-8



NUT_SS_4-40



NUT_SS_4-40



NUT_SS_4-40



NUT_SS_4-40



RUBBER BUMPER



RUBBER BUMPER



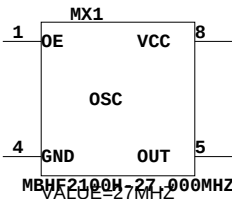
RUBBER BUMPER



RUBBER BUMPER



USB Mini-B Cable



Half Size Oscillator

MJB1



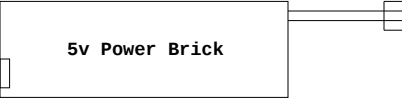
JUMPER_BLOCK_2-PIN

MJB2



JUMPER_BLOCK_2-PIN

PB1



5v Power Brick

Mechanical Components

Title: Mechanical Components SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date: 10-20-2009_14:56		Ver: C	
Sheet Size: B		Rev: 04	
Sheet 16 of 16		Drawn By BF	